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Article

A Switch-inductor Switched-capacitor Based Ultra-gain Boost Converter: Analysis and Design

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Abstract: A feature known as high-voltage gain conversion is necessary for a number of applications, including photovoltaic (PV) connected systems, UPS, SMPS, and some inverter applications, specifically for the power processing of low-voltage renewable sources. This article makes a suggestion for an ultra-gain boost converter based on a switched-inductor switched-capacitor (SISC) network. Ultra-voltage gain (> 15) and lower voltage stresses across the switches are the main benefits of the proposed converter. Additionally, compared with other high-gain topologies, the number of components decreases. This paper presents a systematic analysis of the proposed ultra-gain boost DC–DC converter along with a comparison to other topologies that have been previously published in the literature. The simulation model confirmed that the efficiency of the proposed topology is 95.23%.

1. Introduction

Switching mode power supplies, which are utilised extensively in the sectors of electric power, communication systems, home appliances, industrial devices, railroads, and aircraft, are generally known to be the foundation of contemporary power conversion technology [1,2]. There have been several different converter topologies put up for consideration. The buck converter and the boost converter both have a straightforward design that contributes to their high level of efficiency. However, owing to the limited voltage gain, their applications are restricted when low or high output voltages are required [3]. This is because of the limitation of the voltage gain.

By using the voltage lift technique, Luo converters can achieve significant voltage gain, but at the same time, topological complexity, cost, volume, and losses rise [4–6]. Despite the complexity of their operating mode, converter construction, and control technique, interleaved configurations can attain wide step-down

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or step-up voltage conversion ratios with minimum voltage stresses [7–10]. With fewer switches, quadratic voltage gain can be attained with the cascade configurations, but their efficiency is low [11, 12]. So as to achieve the deep step-down or step-up voltage gain, various switching networks are also added to the fundamental converters [13–23]. However, this complicates construction and raises costs. In contrast to the converter topologies described earlier, which can only step up or step down voltage, the voltage bucking/boosting converters, which have the ability to regulate output voltage under a wider range of input voltage or load variations, are becoming increasingly popular for use in applications such as portable electronic devices, electronic equipment for automobiles, and other related applications. Researchers are all aware of the drawbacks of the traditional buck-boost converter, which has a simple design and high efficiency. The floating power switch, negative output voltage, low voltage gain, and different input and output currents are some of these problems.

The additional fundamental non-isolated configurations, the Cuk, SEPIC, and Zeta converters, have also been offered. These three have the unique ability to step-down and step-up voltage. Conversely, the limitations of the voltage conversion ratio and other drawbacks of the Cuk, SEPIC, and Zeta topologies, however, cannot be disregarded. The quadratic buck-boost converter, put out in [24], has a single power switch that connects to common ground while also achieving voltage gain of $\frac{D^2}{(1-D)^2}$.In a duty cycle larger than 0.5, the diodes D_1 and D_2 clamp the output voltage to the input voltage, limiting the converter's operation to step-down mode.

A buck-boost converter in [25] that provide positive output voltage, continuous output current, continuous conduction mode (CCM) functioning constantly, and no zero on right-half plane. Sadly, the converter's voltage gain of 2 times the duty ratio isn't high enough or low enough to allow it to operate in a broad range of output voltage. Another innovative buck-boost converter with minimal output voltage ripple, less RF interference, and a single common-ground power switch is proposed in [26]. Although the converter is a seventh-order circuit, it has a complicated design, and neither its input node nor its output node bonds the same ground. Additionally, conversion ratio is still constrained. The thermoelectric generator is used in [27] with a boost-buck cascade configuration that combines two independent converters with a current source and current sink. However, this cascade converter's voltage gain is similarly limited. Due to practical limitations, it is particularly difficult to realise that these converters must operate at extremely high or low duty cycles in order to achieve significant voltage step-up or step-down gain. Therefore, it is crucial and valuable to investigate new boost converter topologies in order to overcome the limitations of the existing ones and suit the growing demands in industrial applications.

This study proposes an ultra-gain boost configuration that is created on a switched-inductor switched-capacitor (SISC) network. The proposed ultra-gain converter has the following benefits such as fewer diodes are used in the switching devices, only 2 active switches are present on the current flow channel in dual topological modes, the voltage stresses on the power devices are reduced, and the assembly can operate more efficiently.

2. Ultra-gain Boost Topology

2.1. Origin of the SISC configuration

To construct the suggested converter's front end cell, 2 power switches (S_1 and S_2) and 2 inductors (L_1 and L_2) were used. By connecting them in parallel to the input supply during the on state, these inductors are able to store energy, and by switching to the off state, they are able to discharge it in series. When looking to boost the voltage output of DC-DC configurations without putting excessive stress on the switches, the switched capacitor cell is a viable choice. There are 2 capacitors (C_1 and C_2) and 2 diodes (D_1 and D_2) in this unit. When used with active switches, diodes have the opposite effect. When the

diodes are in a forward bias, the capacitors are charged in parallel and discharged in series. The suggested converter also includes a low-frequency output LC filter, which works to smooth down the output voltage. The resulting arrangement is seen in Fig. 1. The analysis is simplified by considering the aforementioned assumptions.

1. Each component, including the switches and diodes, is lossless.
2. All of the capacitors are of sufficient size, and it is believed that their voltages are constant.

Other findings include the average capacitor currents and inductor voltages being zero for steady state condition. The topology that was designed can function in continuous conduction mode (CCM). These are the operating modes:

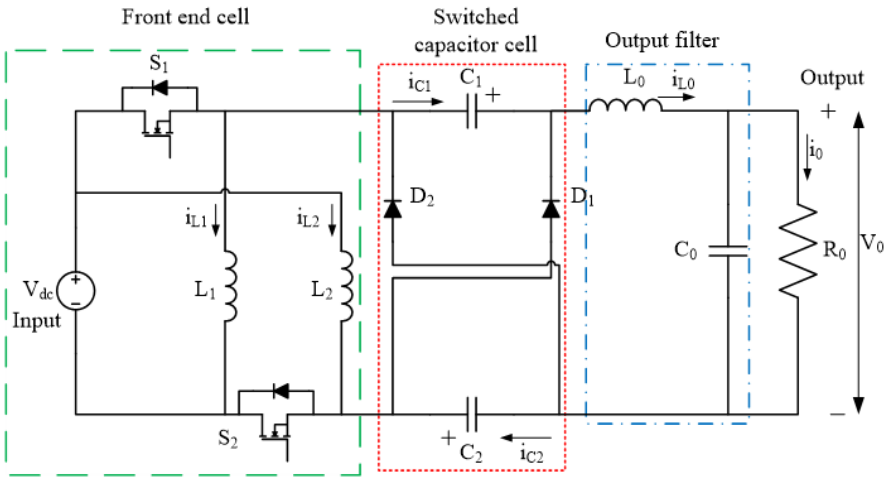

Figure 1. Circuit of proposed ultra-gain boost DC-DC configuration

2.2. CCM Working

The suggested converter under CCM has two working modes during one switching period based on the aforementioned hypotheses.

- State – '1' or Switch ON state.
- State – '0' or Switch OFF state.

Fig. 2 displays the essential waveforms for CCM functioning during one switching period. The following is a description of the operation modes:

2.2.1. State – '1' $(t_0 - t_1)$

The power switches S_1 and S_2 are both triggered at the same period in this mode. The capacitors C_1 and C_2 are discharged in series path during this period, while the D_1 and D_2 diodes are reverse biased. Conversely, the inductors L_1 and L_2 are charged in parallel using the input Vdc. The load is driven by the power lastly stored in capacitors C_1 and C_2, as well as energy from the input. It is possible to express the voltage across the inductors as,

$$V_{L1} = V_{L2} = V_{dc} \ , \tag{1}$$

$$V_{L0} = V_{dc} + 2V_C - V_0 \ . \tag{2}$$

The magnitudes of the inductor voltage for the desired output of the suggested boost DC-DC converter can be calculated using the aforementioned Equations (1) and (2). Fig. 3 depicts the corresponding circuit arrangement for Mode – '1'.

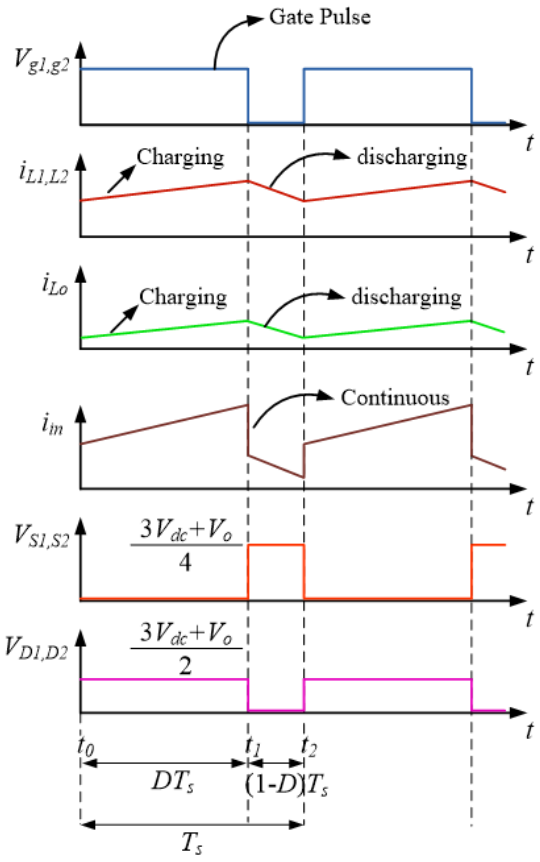

Figure 2. The essential steady state waveforms of proposed boost network: CCM condition.

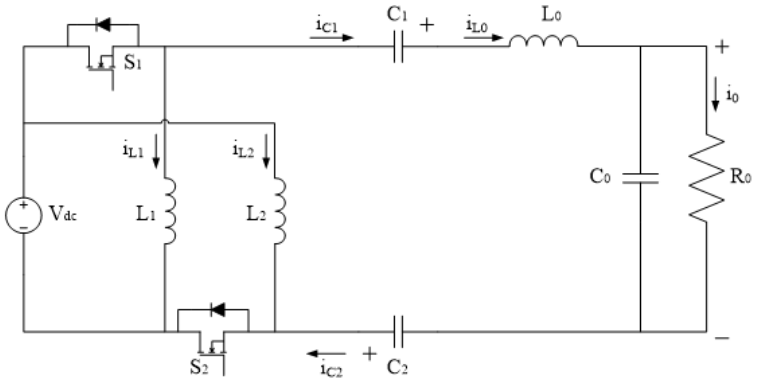

Figure 3. Corresponding network of ultra-gain boost DC-DC topology in state – '1'.

2.2.2. State – '0' $(t_0 - t_1)$

The D_1 & D_2 diodes are forward biased with the active switches (S_1 and S_2) being blocked instantaneously. The voltage source V_{dc} is linked in series with the inductors L_1 and L_2, which supply power to energize the capacitors C_1 and C_2, which are connected in parallel, as well as the output load. It is possible to express the inductors voltage as,

$$V_{L1} = V_{L2} = \frac{V_{in} - V_c}{2} \ , \tag{3}$$

$$V_{L0} = (V_C - V_0) \ . \tag{4}$$

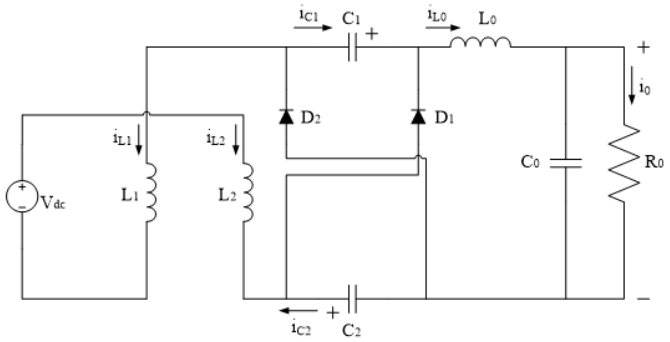

Figure 4. Corresponding network of ultra-gain boost DC-DC topology in state – '0'.

2.2.3. Voltage Conversion Ratio

By applying the volt-second balance technique on the inductors to derive Equation (5) from Equations (1) and (3), and obtaining Equation (6) from Equations (2) and (4), respectively, we get:

$$V_{L1} = V_{L2} = V_{dc}D + (\frac{V_{dc} - V_C}{2})[1 - D] \tag{5}$$

$$V_{L0} = (V_{dc} + 2V_C - V_0)D + (V_C - V_0)[1 - D] \tag{6}$$

From the equations above, the voltage of the capacitors C_1 and C_2 can be calculated as follows,

$$V_{C1} = V_{C2} = V_C = \frac{V_0 - V_{dc}D}{1 + D} \ . \tag{7}$$

From (5), (6), and (7) Equations, the voltage gain M (D) of the ultra-gain boost circuit in CCM condition for a given duty ratio D can be derived as,

$$M_{CCM} = \frac{V_0}{V_{dc}} = \frac{1 + 3D}{1 - D} \ . \tag{8}$$

3. Component design equations and stresses

3.1. Voltage stress on the switches and diodes

If we assume that the current flowing through the capacitors $C = C_1 = C_2$ is equal to the current flowing through the output inductor iL0, we can define the voltage ripple on each capacitor as well as its individual

capacitance. It is possible to rewrite the input voltage as a function of the average voltage V_C across the capacitors as follows:

$$V_C = V_{C1} = V_{C2} = \frac{V_{dc}(1+D)}{1-D} \ . \tag{9}$$

The following are the voltage stresses on switches and diodes:

$$V_S = V_{S1} = V_{S2} = \frac{V_{dc}}{1-D} \ , \tag{10}$$

$$V_{S2} = \frac{V_{dc}}{1-D} \ , \tag{11}$$

$$V_D = V_{D1} = V_{D2} = \frac{2V_{dc}}{1-D} \ , \tag{12}$$

$$V_{D2} = \frac{2V_{dc}}{1-D} \ . \tag{13}$$

With the same input voltage, the proposed DC-DC converter's switch S_1 and diode D_1 experience the same voltage stresses as the power switches in a traditional boost converter, and the diodes in a traditional boost converter experience the same voltage stresses as switch S_2 and diode D_2 in the presented DC-DC converter.

3.2. Inductor design

The inductor voltage (V_L), duty ratio (D), switching frequency (f_S), and ripple current (i_L) all have a role in the final inductor choice [5]. Stage '1' has input inductances L_1 and L_2 at voltages of Vdc. Thus, the values of L_1, L_2, and L0 inductance derived from,

$$L_1 = \frac{V_{dc}D}{\Delta i_{L1} f_s} \ , \tag{14}$$

$$L_2 = \frac{V_{dc}D}{(1-D)\Delta i_{L2} f_s} \ , \tag{15}$$

$$L_0 = \frac{2V_{dc}D}{\Delta i_{L0} f_s} \ . \tag{16}$$

For $D = 0.7419$, $V_{\mathrm{dc}} = 24\,\mathrm{V}$, $f_{\mathrm{S}} = 50\,\mathrm{kHz}$, $\Delta i_{L_1} = 0.8\,\mathrm{A}$, and $\Delta i_{L_2} = 0.8\,\mathrm{A}$. The values of L_1, L_2, and L_0 are given by $L_1 = 445.14\,\mu\mathrm{H}$, $L_2 = 445.14\,\mu\mathrm{H}$, and $L_0 = 1.425\,\mathrm{mH}$.

3.3. Capacitor design

With the voltage ripple present across capacitors C_1, C_2, and C_0, the values of the capacitors may be determined by measuring the variance in their charges [5, 24]. Therefore, we can determine the values of C_1, C_2, and C_0 using the following equations:

$$C_1 = \frac{P_0 D(1-D)}{V_{dc} f_s (1+3D)\Delta V_c} \ , \tag{17}$$

$$C_2 = \frac{P_0 D(1-D)}{V_{dc} f_s (1+3D)\Delta V_c} \ , \tag{18}$$

$$C_0 = \frac{V_{dc}D}{4L_0(f_s * f_s)\Delta V_{C0}} \ . \tag{19}$$

For $D = 0.7419$, $V_o = 300\,\text{V}$, $f_S = 50\,\text{kHz}$, $\Delta v_{c_1} = 5\,\text{V}$, and $\Delta v_{c_2} = 5\,\text{V}$. The values of c_1, c_2, and c_0 are given by $c_1 = 4.95\,\mu\text{H}$, $c_2 = 4.95\,\mu\text{H}$, and $c_0 = 1.25\,\text{mH}$.

3.4. Current stress on the switching elements

The input power and output power are considered equal i.e.:

$$P_{in} = P_0 \ , \tag{20}$$

$$V_{in}I_{in} = V_0 I_0 \ . \tag{21}$$

The currents are given as,

$$\frac{I_{in}}{I_0} = \frac{1-D}{1+3D} \ . \tag{22}$$

From ohm's law,

$$V_0 = I_0 R \ . \tag{23}$$

Applying the ampere-second balance rule on output filter capacitor C_0, we get,

$$I_{L0} = I_0 \ . \tag{24}$$

The DC currents I_{L1}, I_{L2}, I_{in} and I_0 are given as,

$$I_{in} = (2I_L + I_{L0})D + I_L(1-D) \ , \tag{25}$$

$$I_0 = \frac{1-D}{1+3D} I_{in} \ . \tag{26}$$

From Equations (6), (9), (20), (21) and (22), we get,

$$I_{L1} = \frac{P_0(1+D)}{V_{in}(1+3D)} \ , \tag{27}$$

$$I_{L2} = \frac{P_0(1+D)}{V_{in}(1+3D)} \ . \tag{28}$$

The current stress equations of active and passive switches are listed as:

$$I_{S1} = \frac{2P_0\sqrt{D}}{V_{in}(1+3D)} \ , \tag{29}$$

$$I_{S2} = \frac{2P_0\sqrt{D}}{V_{in}(1+3D)} \ , \tag{30}$$

$$I_{D1} = \frac{P_0(1-D)}{V_{in}(1+3D)} \ , \tag{31}$$

$$I_{D2} = \frac{P_0(1-D)}{V_{in}(1+3D)} \ . \tag{32}$$

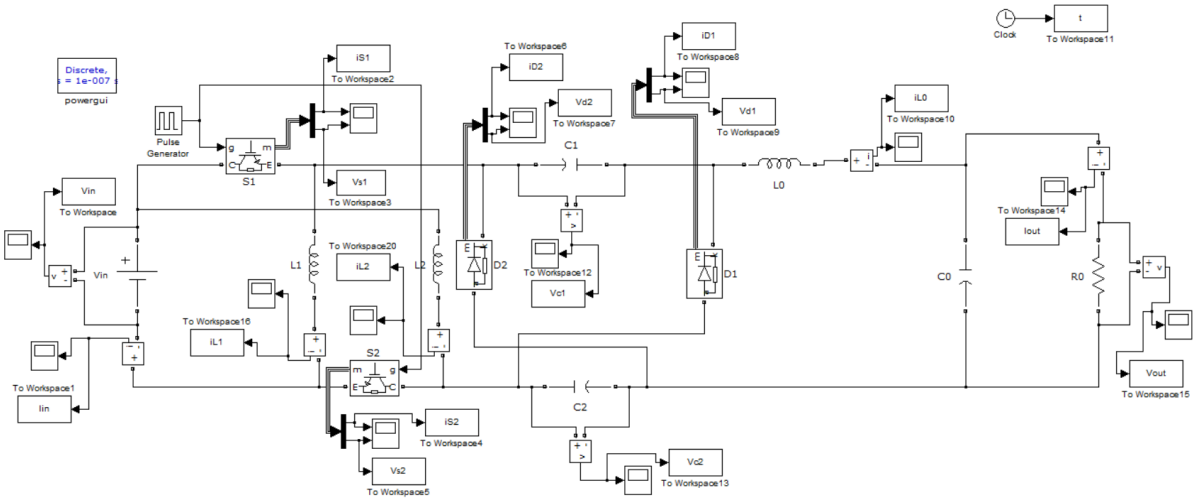

Figure 5. Simulink model of designed ultra-gain DC-DC converter.

From the above Equations (29), (30), (31) and (32) the current stresses of power switch S_1,S_2 and diode D_1,D_2 are equal to each other and the power switches current of traditional DC-DC converters are also same so the currents across the diodes are equally divided in the proposed converter.

4. Discussion on results

This section describes the ultra-gain DC-DC boost converter's simulink model, which actually proves the specified goals by presenting the converter's detailed waveforms. The circuit components taken into account by the MATLAB simulation are shown in Table 1. For the purpose of presenting this DC-DC converter, these theoretical values were used in the calculations. With a 24V input, a 300V output is to be expected. We assume a load resistance of 180 ohms and a switching frequency of 50 KHz, yielding an output power of 500W. The duty cycle, D = 0.7419, is derived from the voltage conversion ratio, $M(D)$. To simplify, let's assume that the ripple currents in inductors L_1, L_2, and L_0 are 0.8A, 0.8A, and 0.5A, respectively, for capacitors C_1 and C_2. To simplify, let's say that the ripple voltage is 5V and the C_0 is 3V. Inductors (L_1, L_2, and L_0) and capacitors (C_1, C_2, and C_0) may be determined using the equations shown above.

Table 1. Simulated circuit parameters for proposed DC-DC converter.

Components	Values
Input voltage (V_{dc})	24 V
Output voltage (V_0)	300 V
Switching frequency (f_S)	50 kHz
Output power (P_0)	500 W
Output load (R)	180 ohms
Duty ratio (D)	0.7419
Voltage gain $(M(D))$	12.5
Filter Inductor (L_0)	1.425 mH
Input Inductors $(L_1 = L_2)$	445.14 µH
Intermediate Capacitors $(C_1 = C_2)$	4.95 µF
Filter Capacitor (C_0)	1.25 µF

Table 2. Proposed configuration performance with ripple and efficiency

S.no	Duty ratio (D)	Pin (W)	Output Voltage (V0)	P0 (W)	% Ripple	% Efficiency
1	0.10	6.59	33.62	6.28	0.24	95.23
2	0.15	9.17	39.63	8.73	0.33	95.17
3	0.20	12.58	46.40	11.97	0.32	95.11
4	0.25	17.09	54.07	16.24	0.31	95.02
5	0.30	23.09	62.83	21.94	0.36	95.02
6	0.35	31.13	72.95	29.57	0.34	95
7	0.40	42.05	84.75	39.90	0.29	94.90
8	0.45	57.05	98.70	54.11	0.20	94.85
9	0.50	78.09	115.40	74	0.26	94.76
10	0.55	108.31	135.90	102.60	0.29	94.73
11	0.60	153.05	161.50	144.86	0.31	94.65
12	0.65	221.95	194.30	209.84	0.15	94.55
13	0.70	333.84	238.20	315.14	0.17	94.11
14	0.74	503.76	293.20	474.69	0.17	94.23
15	0.75	529.20	299.50	498.36	0.16	94.17
16	0.80	907.20	391.40	850.90	0.10	93.80

The ultra-gain DC-DC converter simulink model is shown in Fig. 5. Two switches, three inductors, two diodes, three capacitors, a load resistance, and a power supply input are needed to create the suggested converter. Both switches are concurrently coupled to one other, therefore only one pulse generator is required. The workspace is added to the scopes, and the voltage and current measurements are connected to the necessary Simulink components so that the desired graphical waveforms may be obtained.

Table 2 displays the input power, output voltage, output power, % ripple, and efficiency of the proposed ultra-gain DC-DC converter for a range of duty ratios. For duty ratios between 0.1 and 0.8, the values are calculated. The simulated output voltages are nearly matching the theoretical values (Equation (8)) allowing some device voltage drops. The ripple factor is very small which is under 0.5% with smaller output capacitance value of 1.25µF. Hence the size and cost the of the converter cuts down to a margin. The respective efficiency values are also evaluated using the simulation model. Even at very low duty ratios (say 0.1), very high efficiencies (> 95%) are obtained. During the entire range of duty ratios the efficiency ranges between 93-96% with a highest efficiency of 95.23%. The Table 3 determines the voltage stresses of switches and diodes with various duty ratio (Equations (10) – (13)). From table 3 it can be witnessed that the active & passive switch voltage stresses are very less than the output voltages. Thus, resulting in lower switching losses, higher efficiencies with less device ratings.

Table 3. Voltage stresses of switches and diodes for various duty ratios.

S.no	Duty ratio (D)	Output voltage (V0)	VS	VD
1	0.10	33.62	26.67	53.34
2	0.15	39.63	28.24	56.48
3	0.20	46.40	30	60
4	0.25	54.07	32	64
5	0.30	62.83	34.29	68.58
6	0.35	72.95	36.90	73.80
7	0.40	84.75	40	80
8	0.45	98.70	43.64	87.28
9	0.50	115.40	48	96
10	0.55	135.90	53.33	106.66
11	0.60	161.50	60	120
12	0.65	194.30	68.57	137.14
13	0.70	238.20	80	160
14	0.75	292.30	92.99	185.98
15	0.76	299.50	96	192
16	0.80	391.40	120	240

Fig. 6 denotes the simulated graph of the input voltage of the proposed DC-DC configuration with a continuous input of 24V. Fig. 7 shows the simulated waveform of the output voltage and the value is 293.2V with a ripple of 0.18%, which is nearer to the expected value of 300V at a duty ratio of 0.7419. The above-said calculations are made by using the necessary equations derived from the steady state theoretical analysis given in Sections 2 and 3. The power was taken as 500 W (see Table 1) by considering it as a lossless converter, whereas the simulated output power is obtained as 475W with an input power of 504W (see Table 2) approximately.

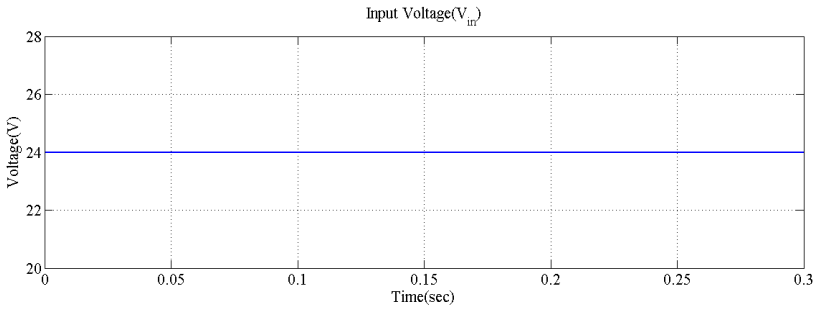

Figure 6. Simulation waveform of input DC voltage – 24V.

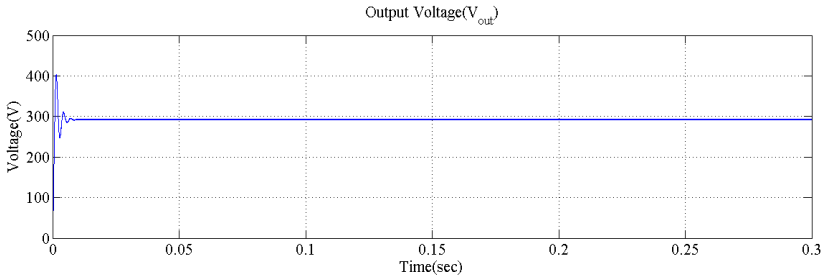

Figure 7. Simulation waveform of DC output voltage.

Fig. 8 represents the simulated waveform of input current of the suggested DC-DC topology. It can be observed that a continuous input current is flowing with an allowable ripple. The average value is obtained as 21A with a peak of 25A approximately. Fig. 9 illustrates the output current waveform of the given topology for the duty ratio of 0.7419. The average output current value is obtained as 1.65A for a load of 180 ohms.

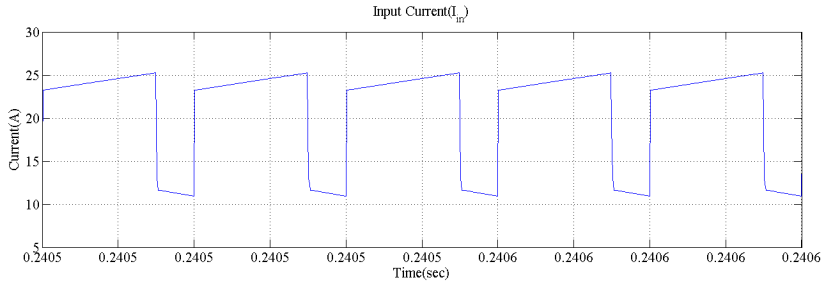

Figure 8. Simulation waveform of input current.

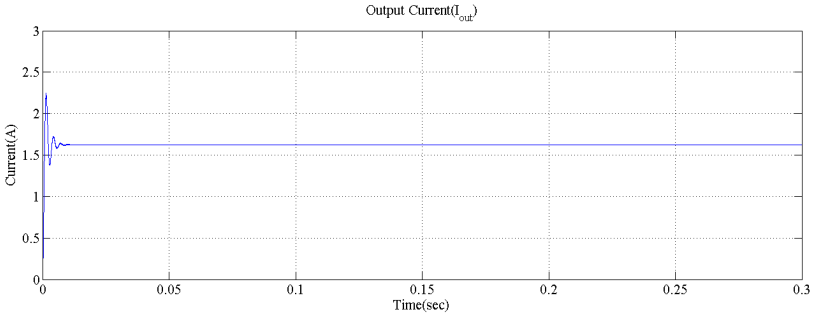

Figure 9. Output current waveform of the simulation.

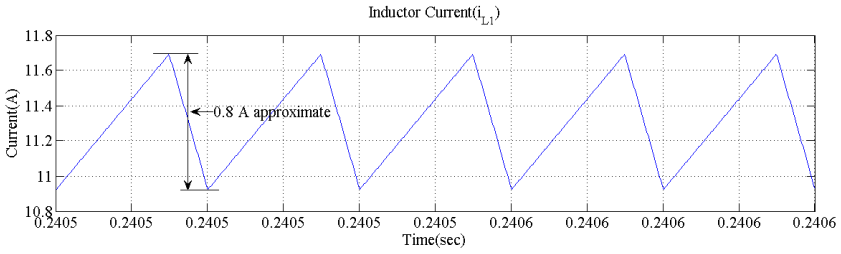

Figure 10. Simulation waveform of inductor L_1 current i_{L1}.

A simulated waveform of inductor L_1 current i_{L1} is illustrated in Fig. 10 of the given configuration. For the designed values, the inductor L_1 current ripple is considered as 0.8A. From Fig. 10, it is proved that the simulated ripple i_{L1} exactly matches the assumed value for the theoretical calculations. The inductor L1 average current value is observed as 11.22A for a duty ratio of 0.7419.

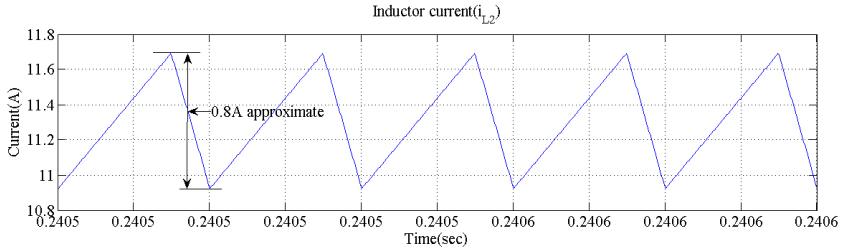

Figure 11. Simulation waveform of inductor L_2 current i_{L2}.

In Fig. 11, simulation waveform of inductor L_2 current i_{L2} is shown. For the designed values, the inductor L_2 current ripple is considered as 0.8A. From Fig. 11, it is verified that the simulated ripple i_{L2} exactly matches the assumed value for the theoretical calculations. The inductor L_2 average current value is observed as 11.22A for a duty ratio of 0.7419.

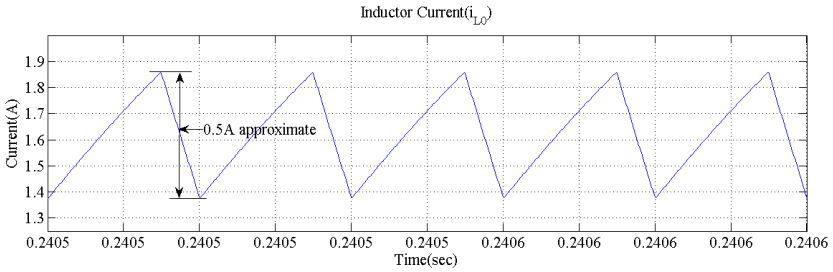

Figure 12. Output inductor current i_{L0} simulation waveform.

In Fig. 12, simulation waveform of output inductor current i_{L0} is shown. The inductor L_0 average current value is observed as 1.5A for a duty ratio of 0.7419. For the designed values, the inductor L_0 current ripple is considered as 0.5A. From Fig. 12, it is proved that the simulated ripple i_{L0} exactly matches the assumed value for the theoretical calculations.

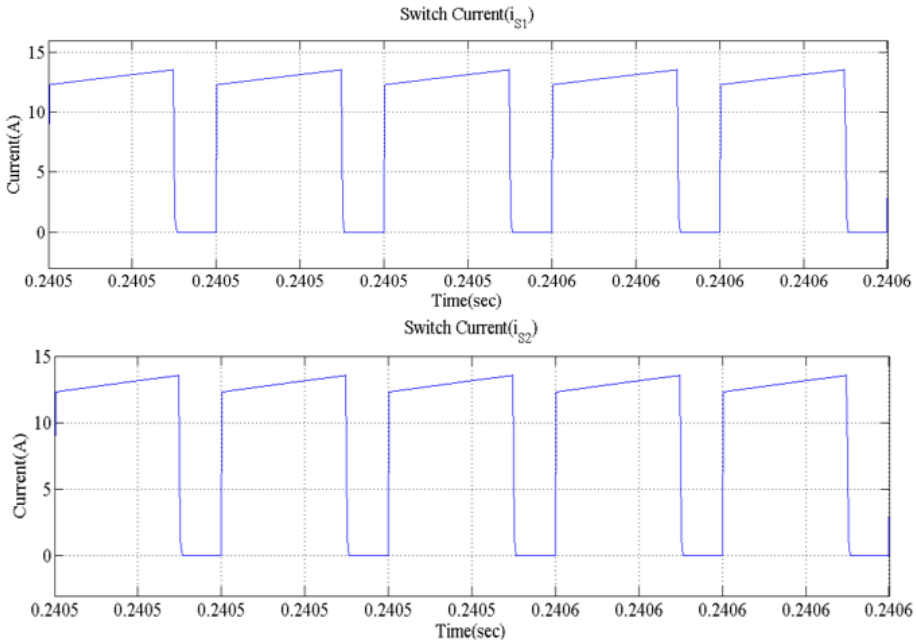

Figure 13. Simulated waveform of active switch currents.

The simulated waveforms of both the active switch currents i_{S1},i_{S2} respectively are shown in Fig. 13 for the suggested DC-DC topology, and the average current values are given as 10.52A for the duty ratio of 0.7419. The waveform is shown for 5 time cycles with the x-axis taken as time for the duration of 0.2405s to 0.240s. It can be witnessed that jointly the switches allows the equal amount of current.

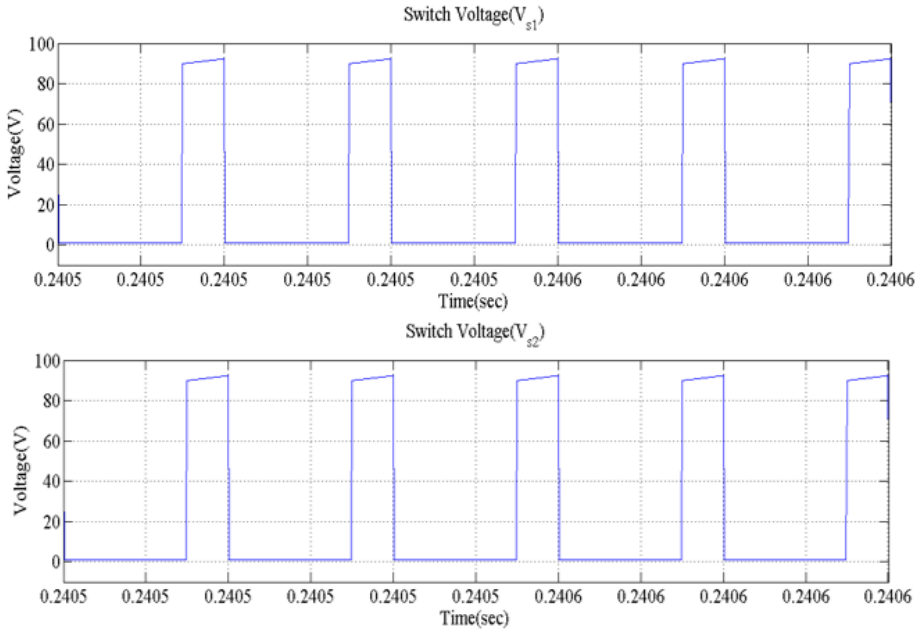

Figure 14. Simulation waveform of active switch voltages.

Fig. 14 demonstrates the simulation waveform of active switch voltages V_{S1},V_{S2} which are around 93.5V peak for the designed duty ratio of 0.7419. The switching stresses of simulated values match the theoretical values which are given in Table 3. The waveform is shown for 5 time cycles with the x-axis taken as time for the duration of 0.2405s to 0.240s. It can be observed that both the switches block the same amount of voltage. From Figs. 13 and 14, it can be seen that both the switches carry current for the duration of 74.19% of TS and block the voltage for the remaining duration.

The simulated waveforms of both the active switch currents i_{d1},i_{d2} respectively are shown in Fig. 15 for the proposed DC-DC converter, and the peak current values are given as 6.8A for the duty ratio of 0.7419. The waveform is shown for 5 time cycles with the x-axis taken as time for the duration of 0.2405s to 0.240s. It can be observed that both the switches allow the equal amount of current. Fig. 16 illustrates the simulated waveform of active switch voltages V_{d1},V_{d2} which are around –180.2V peak for the designed duty ratio of 0.7419. The switching stresses of simulated values match the theoretical values which are given in Table 3. The waveform is shown for 5 time cycles with the x-axis taken as time for the duration of 0.2405s to 0.240s.

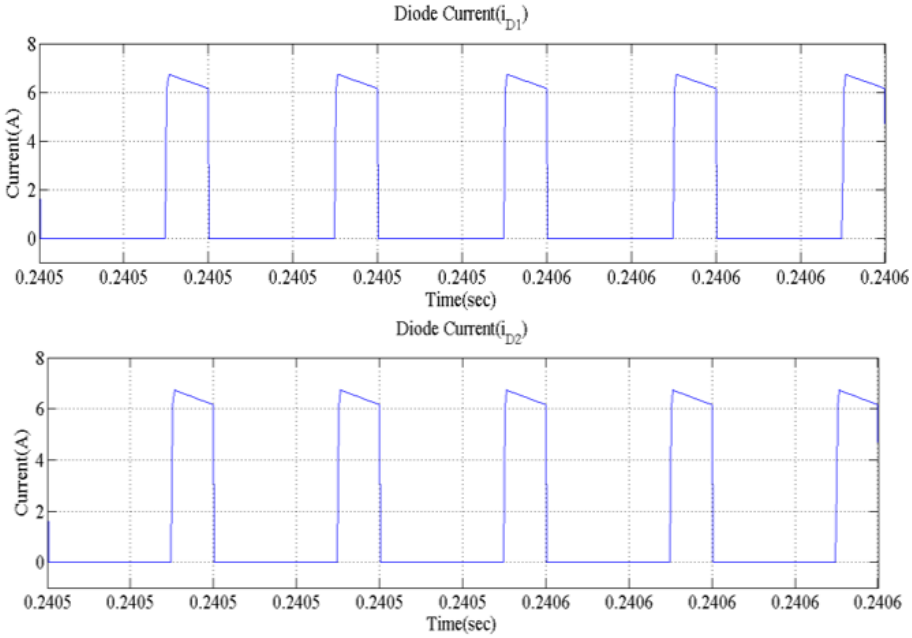

Figure 15. Simulation waveform of diode currents.

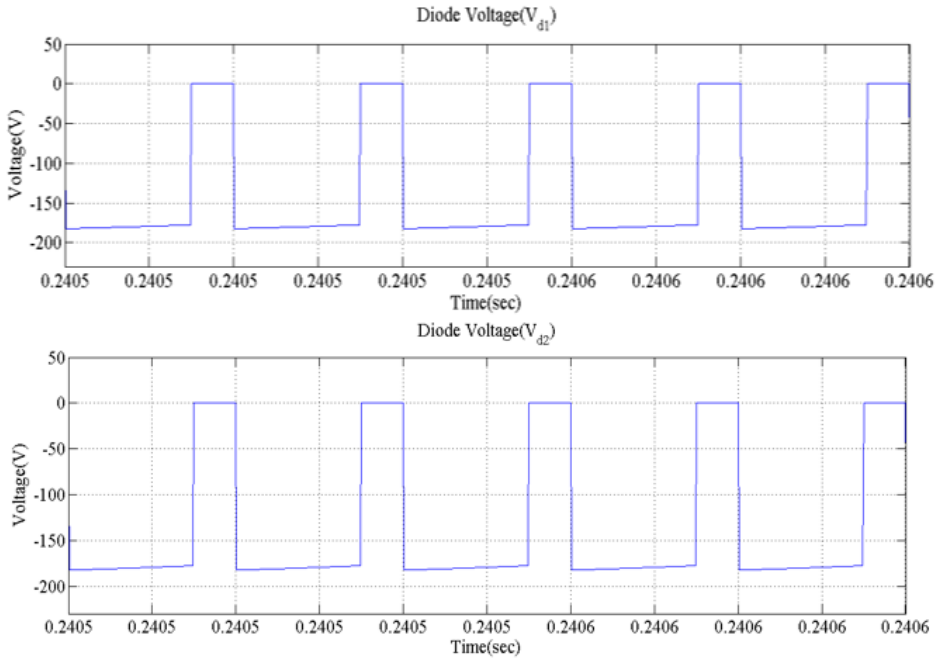

Figure 16. Simulated waveform of diode voltages.

It can be observed that both the switches block the same amount of voltage. From Figs. 15 and 16, it can be seen that both the switches carry current for the duration of 74.19% of TS and block the voltage for the remaining duration.

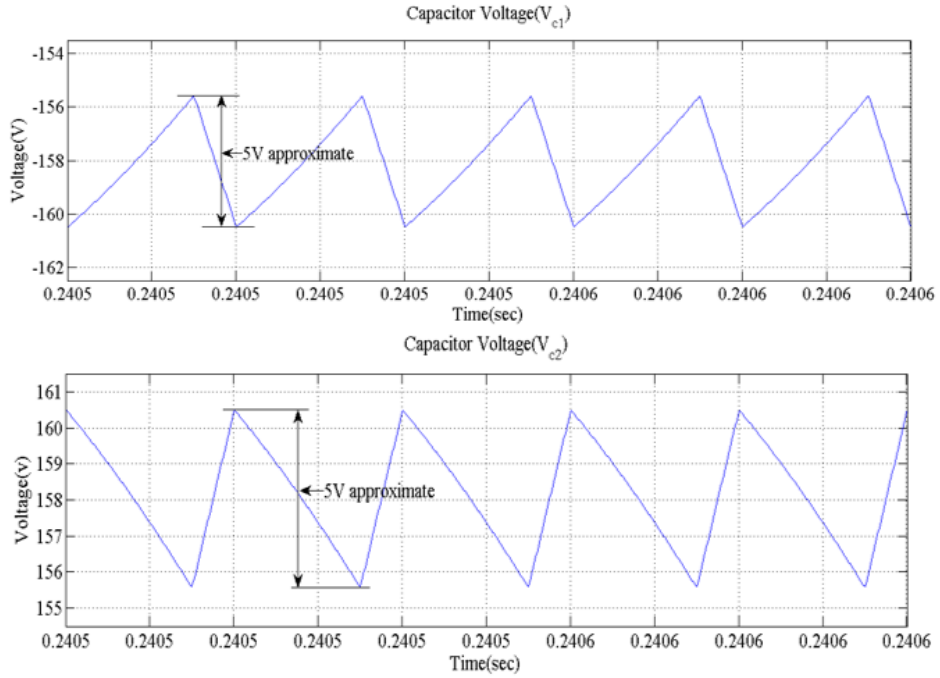

Figure 17. Simulated waveform of capacitor voltages V_{C1}, V_{C2}.

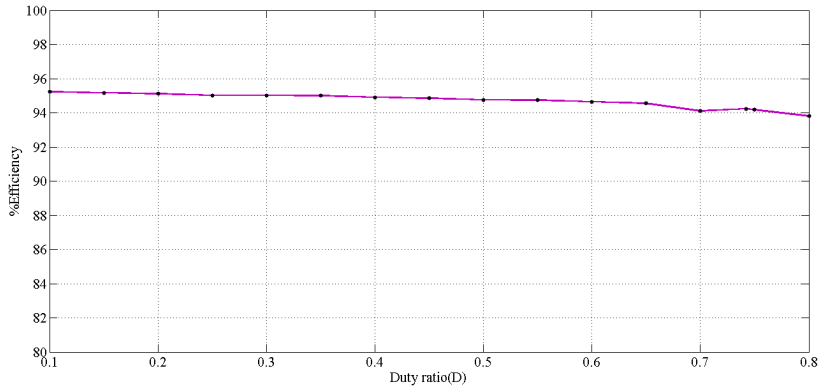

Figure 18. The efficiency plot of the suggested dc-dc topology for several duty ratios.

In Fig. 17, the simulated waveforms of switched capacitor voltages V_{C1}, V_{C2} are illustrated, which are nearly 156.8V. The waveform is shown for 5 time cycles with the x-axis taken as time for the duration of 0.2405s to 0.240s. The charging and discharging cycles of the capacitors are also shown as described in Section 2. During the converter's design, the ripple voltage of both capacitors is assumed to be 5V, which corresponds to the simulations in Fig. 17.

The effectiveness of the proposed configuration is tested for various duty ratios ranging from 10% to 80% (0.1 to 0.8) along with the designed duty ratio value of 0.7419. All the tested simulated values with the corresponding efficiencies are listed in Table 2 for the above-mentioned duty ratios. From table 2, the efficiency curve has been plotted (Fig. 18) for several duty ratios from 0.1 to 0.8. Fig. 18 shows that the proposed converter has worked well for all of the different duty ratios because it has higher efficiencies (more than 93%). The input and output powers of the suggested ultra-gain configuration are calculated

and listed in table 2. From table 2, the input and output powers are plotted, which are shown in Fig. 19. Hence, it can be noted that the gap between the power curves is almost negligible, hence achieving higher efficiencies.

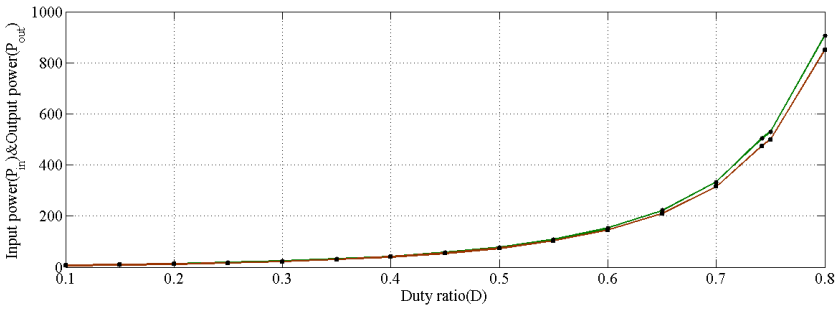

Figure 19. The plot of input and output powers for various duty ratios.

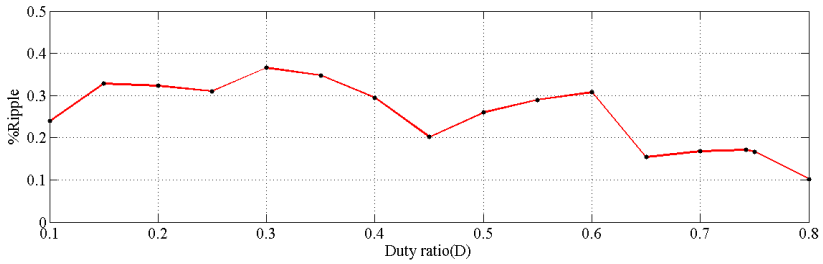

Figure 20. The output voltage ripple factor for various duty ratios.

The calculated output voltage ripple is plotted and shown in Fig. 20 (table 2) for the various duty ratios. It is proved that the % ripple factor is very less, under 0.5%.

5. Comparative view

The suggested topology is contrasted in this section with non-isolated architectures that also offer substantial voltage increases, including the SL-Boost [18], circuit I [21], circuit III [21], hybrid boost converter (HBC) [23], converter [24], and converter [25]. For these converters, the voltage gain and the standardized equations that characterize the voltage stresses across the switching elements are visually depicted in Figs. 21 and 22, respectively, and are summarized in Table 4. Table 4 also displays the total components count used in each of the examined configurations. With only single power switch and hence a simple driver circuit, the configurations [18], [23], and [25] offer the equivalent voltage gain as converters – I and III [21], and [24], respectively. The HBC[23] is a fascinating topology when the amount of components is taken into account, especially given that it is equivalent to the circuit III [21] in terms of voltage gain and stress on the devices. The HBC [23] has an advantage over the suggested converter in terms of the quantity of active switches and inductors, but Fig. 21 shows that the proposed converter utilises few capacitors and diodes and can give greater voltage gain for duty ratios above 0.5. As illustrated in Fig. 22, the suggested configuration also reduces the voltage stress on power switching elements for any voltage gain above 5.

Table 4. Comparative view of various step – up converters with the proposed model.

References	[18]	[20]	Circuit – I [21]	Circuit – III [21]	[23]	[24]	[25]	Proposed
SC	1	2	2	2	1	2	1	2
DC	4	7	1	3	4	3	3	2
IC	2	4	2	2	1	2	1	3
CC	1	1	1	3	4	3	3	3
TC	8	14	6	10	10	10	8	10
DS = $\frac{V_D}{V_{dc}}$	$\frac{1+D}{1-D}$	$\frac{D}{1-D}$	1	$\frac{2(1+D)}{1-D}$	$\frac{D}{1-D}$	$\frac{2}{1-D}$	$\frac{1}{1-D}$	$\frac{1+D}{2(1-D)}$
SS = $\frac{V_S}{V_{dc}}$	$\frac{1+D}{1-D}$	$\frac{1+D}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1+D}{2(1-D)}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$
M(D) = $\frac{V_0}{V_{dc}}$	$\frac{1+D}{1-D}$	$\frac{1+3D}{1-D}$	$\frac{1+D}{1-D}$	$\frac{3-D}{1-D}$	$\frac{3-D}{1-D}$	$\frac{2}{1-D}$	$\frac{2}{1-D}$	$\frac{1+3D}{1-D}$
ICR	Less	More	More	More	More	Less	Less	More

* *SC – Switch Count, DC – Diode Count, IC – Inductor Count, CC – Capacitor Count, TC – Total Count, M (D) – Voltage Gain, SS – Switch Stress, DS – Diode Stress & ICR – Input Current Ripple.*

The newly reported converter [24] has the same input current characteristics as the proposed topology and have a need of the similar elements. However, for any duty ratio above 0.333, [24] provides a lower static gain, and for the voltage gain more than 5, their power switches are exposed to maximum voltage stress. As shown in Fig. 22, the topologies [21] and [18] have the lowest voltage gains when compared, and their power switches experience higher voltage stresses, particularly [18]. Table 4, taking into account the topological derivation of each converter, displays the normalised voltage stresses on the diodes (V_D/V_{dc}). Additionally, the diodes that involve the combination of the suggested converters, HBC [23], configuration [24], and SC-Boost [25], evenly distribute the voltage stress.

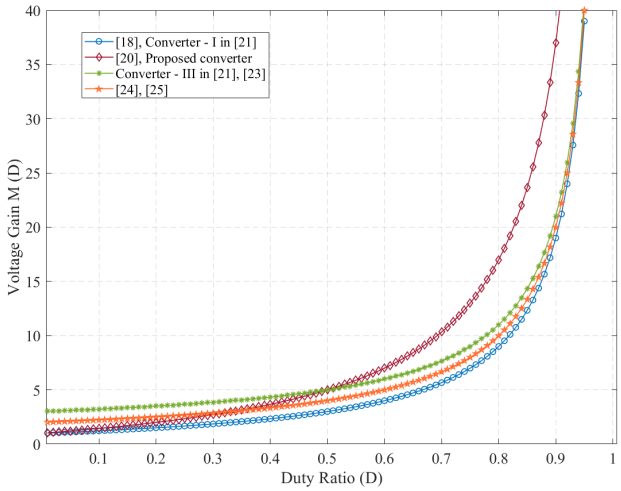

Figure 21. Voltage gains assessment of step-up configurations with the given model.

The proposed and SH-SLC [20] converters can be compared specifically since they both have the same voltage gain and achieve the highest values among the compared converters, as shown in Table 4 and Fig. 21. When compared to the SHSLC, the proposed configurations total component count is lower, despite the addition of two non-high capacitance film capacitors [20] (five diodes and one inductor less). Furthermore, for any duty ratio more than 0.5, Table 4 and Fig. 22 show that the suggested configuration provides the largest voltage gain and the lower voltage stresses on the active switches. This feature makes

it possible to employ switches with lower "ON" resistances, which lowers conduction losses. There are various modern coupled inductors and interleaving topologies that can have input current sharing and also attain higher gains, even with the comparison study only including related configurations to the suggested topology. These converters (and others built on the same ideas) feature low input current ripple and can have their voltage gain changed by the turn's ratio. They do, however, have higher component counts and more sophisticated structures and analysis designs.

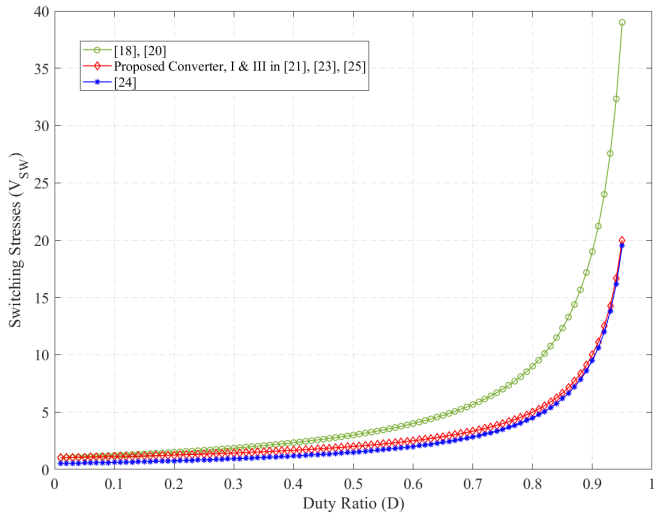

Figure 22. Voltage stresses assessment of step-up configurations with the suggested model.

6. Conclusions

An ultra-gain boost DC-DC configuration is suggested in this work. The newly developed converter is straightforward, and modifying the DC-DC configuration simply requires the addition of six parts. Numerous benefits of the suggested converter include its input current continuity, very high gain, non-inverting output voltage, and straightforward control scheme. Moreover, linked inductors and transformers are not used to produce the extremely high voltage gain. Because of this, there is no voltage overshoot across the switches, negating the requirement for a clamping circuit. With minimum switching voltage stresses and lower Rds (on), this effect lowers conduction losses and enables an added compact system. The converter's steady-state studies under CCM operation and design factors have been reported. The suggested configurations switches voltage stress, high voltage gain, and element count are assessed with several other recent step-up configurations. The voltage gain is more of the suggested converter than the other topologies, per the results that have been reported. Also, compared to the output voltage, stresses on the switches are less for the suggested topology.

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