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Article

A Novel Switched-Capacitor Enhanced-Boost Quasi Z-Source Network

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Abstract: This paper presents a novel switched-capacitor enhanced-boost quasi-Z-source inverter (SCEB-qZSI) for renewable energy applications. The described topology is a novel power electronic converter that uses switched-capacitors to increase the voltage boost. In the meanwhile, a reduced shoot-through condition results in a higher dc-link voltage. Moreover, the proposed concept has the advantages of continuous input current, smaller current ripple, common grounding, and high output voltage gain. The proposed topology is thoroughly examined, and simulation data are used to support the theoretical analysis. The proposed SCEB-qZSI topology has potential uses in electric vehicles, industrial applications, and renewable energy systems which may develop by using the inexpensive components making it an attractive option for applications that have limited funds. D represents the shoot-through duty ratio of the inverter switches which can range from 0<D<0.144. In the proposed topology inductor voltages, inductor currents, capacitor voltages, diode currents, and voltage source inverter outputs are extracted with and without filters and are discussed in brief. The theoretical and simulation evaluation for the above findings is presented in this paper.

1. Introduction

There is a rising tendency towards the usage of renewable energy resources as a result of the rapid depletion of fossil fuel supplies and the environmental problems brought on by their use. Photovoltaic systems, which provide electricity from sunshine, are one of the most promising forms of renewable energy. However, solar panels often provide a low DC output voltage, which is inappropriate for many power applications [1]. In order to increase the output voltage of solar panels to a level that can be used for power applications, efficient and effective DC-DC converters are required. The typical converter voltage source inverter (VSI) only has the ability to perform buck operations, and thus it is mostly employed in renewable energy systems [2]. Buck converters that work with DC-DC power sources will provide low output voltage.

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The size and efficiency of the converter are both impacted by the two-stage conversion. Voltage source inverters (VSIs) are often utilized in power conversion applications. However, they can be vulnerable to electromagnetic interference (EMI) noise and gating pulse mismatches, which can result in a short-circuit in the input voltage source. The VSI switching pattern can be modified to include a dead period, which can prevent the EMI noise and gating pulse mismatches.

Inverter bridge can use the shoot-through (ST) interval by using the impedance (Z) network to increase the voltage gain. During this period, all the switches in the inverter bridge are turned on. By including an impedance network, Z-Source Inverters (ZSIs) can harness the ST state's advantages, such as its capacity to enhance output voltage and improve dependability against input voltage source short-circuits. Minimal dead time can lead to better output waveform quality, increased operating efficiency, and reduced power losses during switching. [3]. The usage of ZSIs in DC-AC power conversion applications utilizing modulation techniques has resulted in the development of several topologies due to these characteristics. Despite having various advantages, the ZSI has a number of disadvantages are also presented, which should be taken into account. These disadvantages include reduced switching losses, which can lead to lower efficiency and higher power losses, discontinuous input current, and no common grounding between input and output [4].

By adjusting or replacing Z-network individual parts, which may be implemented as the quasi-Z- source inverter (qZSI) [5]. The total benefit will be same for both ZSI and qZSI. In renewable energy systems that require a wide variety of voltage increases, the qZSI can pose a serious difficulty. The need for higher shoot-through intervals, which can result in significant voltage stress on the semiconductors of the H-bridge inverter, is one of the difficulties with both ZSI and qZSI. This may result in a low modulation index, poor output voltage quality and decreased efficiency. While the qZSI is an improvement over the traditional ZSI, further modifications may be necessary to achieve higher voltage gains and enhanced performance.

There are several Z-source inverter (ZSI) topologies that achieve a significant voltage boost factor by using switched-inductor (SL) cells to create SL-ZSIs, which is one method for enhancing the voltage gain of conventional ZSIs and qZSIs. This approach has demostrated to further improve the boost capabilities [6]. This topology's structure includes a voltage-lifting unit [7].

Additionally, extended-boost passive parts and diodes are employed to increase the output voltage gain range of the qZSI. There are two distinct arrangements for these parts: capacitor/diode aided ZSI [8–10].

The suggested qZSIs provide the same voltage gain as the traditional ZSI, along with the added advantage of conserving one L-C pair. But, doing so necessitates adding a second active switch and a second diode to the circuit. To increase the system's voltage gain, many ZSI topologies have been proposed. One such topology is the Enhanced-boost Z-source inverter (EB-ZSI), which uses two switching impedance networks to provide a higher gain. The EB-ZSI requires a shorter ST period than other ZSIs, like the diode-assisted z-source network (DA-ZSN) and switched-inductor z-source network (SL-ZSN), to obtain the same voltage gain, which lowers conduction losses and improves output waveform quality [11]. However, the EB-ZSI has limitations, including a discontinuous input current and several ground points. These limitations can be addressed by effectively cascading the qZSI and keeping the same boost capability with the same number of circuit components [12].

The enhanced-boost active-switched quasi-Z-source inverter (EB-ASqZSI) topology uses two fewer L-C pairs than the EB-qZSIs to provide the same voltage gain. In a similar manner, the active-switched inductor boost quasi-Z-source inverter (ASLB-qZSI) obtains a voltage gain comparable to that of the EB-qZSIs with one fewer L-C pair and one additional active switch [13]. However, both of these topologies put significant voltage stress on semiconductors and require an extra isolated gate driver, which can raise system costs.

A novel switched-capacitor enhanced-boost quasi-Z-source inverter (SCEB-qZSI) was proposed in [9]. This inverter works by incorporating a switched-capacitor cell in the inverter's impedance network, which increases the efficiency and allows a greater voltage boost factor. The switched-capacitor cell is frequently

switched during SCEB-qZSI operation in order to move energy from the input to the output. As a result, the voltage gain may increase without extending the ST time, reducing conduction losses and enhancing the quality of the output waveform. Additionally, the inverter has a constant input current mode that may be used to increase system stability and minimize current ripple. Compared to the traditional qZSI, the SCEB-qZSI provides a greater voltage boost, increased efficiency, and improved output waveform quality. It keeps the benefits of qZSI, including common grounding for the input and output, and it has continuous input current. Additionally, because of its smaller size, it offers a better power density. For renewable energy systems and other applications that need a significant voltage gain, it is a potential alternative.

The capacitor-switched type Z-source inverter is a promising technology for power conversion applications. It uses a unique impedance network that allows to boost the input voltage and handle a wide range of input voltages. The addition of capacitor-switched circuits to the Z-source inverter topology enhances its functionality and performance, by providing a more flexible and efficient way to manage the flow of energy.

The introduction to different configurations of Z-network topologies is elaborated in Section 1. Section 2 describes the operating principle of the proposed inverter topology as well as derivations of capacitor voltages, inductor current, and diode voltages. Section 3 describes the parameter design of the Z-network. Discussion on simulations and verifications with theoretical values are explained in Section 4. Finally, Section 5 presents the concluding remarks.

2. The Proposed Topology

In order to achieve the boost performance with a better power density, the capacitor C_3 is parallel to the inductor L_2, differing from the previous design (SC-EBqZSI) shown in Figure 1. This modification results in a boost factor three times the input voltage for a specified duty ratio (D) and input voltage. The switched-capacitor (SC) idea is used in this topology. However, it has a lower boost factor than the SC-EBqZSI.

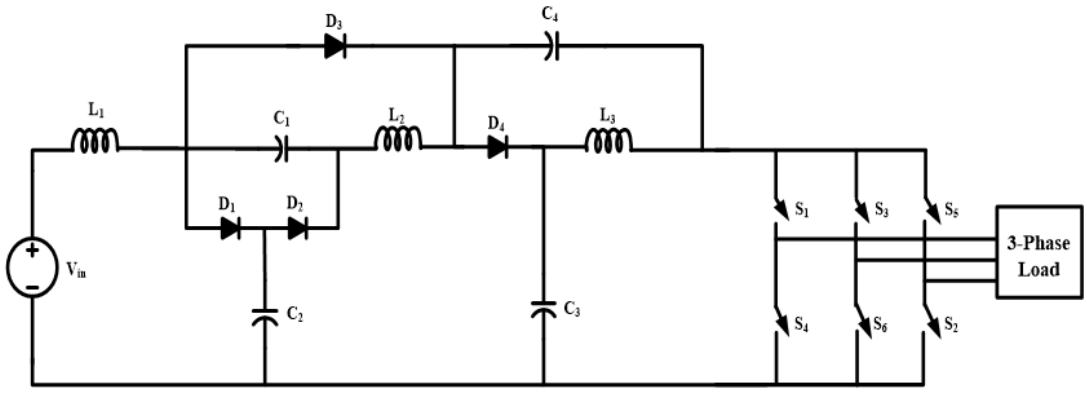

Figure 1. Circuit configuration of enhanced-boost switched-capacitor quasi-Z-source inverter [9].

Figure 2 presents the circuit diagram of the proposed topology, which consists of three inductors, four capacitors, and four diodes. This topology has the same components as the previous topology but reduces stresses on capacitors and the complexity of the design.

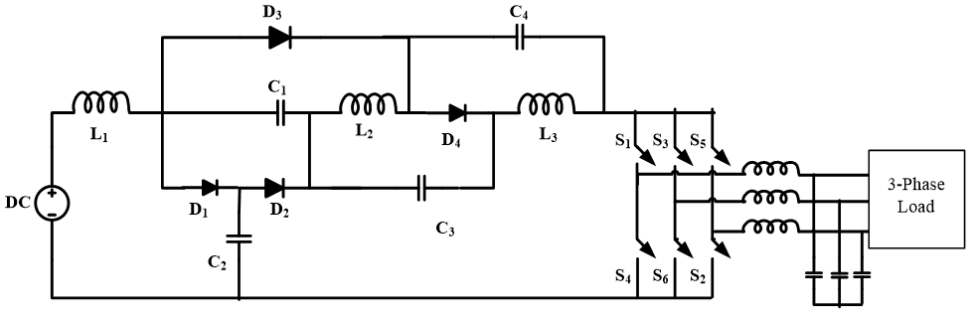

Figure 2. Circuit configuration of the proposed novel switched-capacitor enhanced-boost quasi-Z-source inverter topology.

The proposed topology operates in two states: shoot-through (ST) and non-shoot-through (NST). These states are depicted in Figures 3(a) and 3(b), respectively.

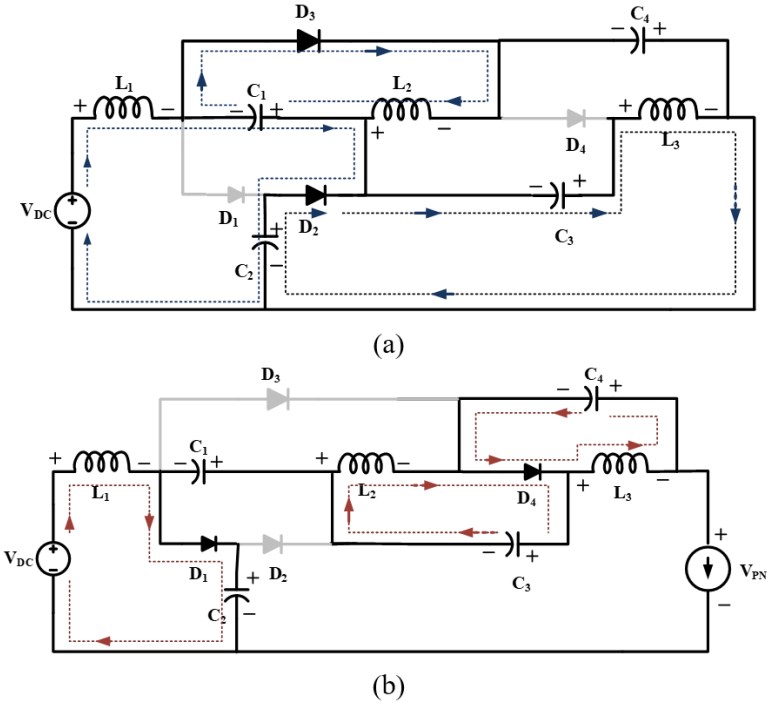

Figure 3. Equivalent circuit diagram for the proposed topology in (a) shoot-through mode and (b) non-shoot-through mode of operation.

2.1. Shoot-through State

Figure 3(a) represents the shoot-through state of the converter. As a consequence, diodes D_2 and D_3 are in forward-biased condition and are in the ON state, whereas diodes D_1 and D_4 are in reverse-biased condition and are in the OFF state. Simultaneously, capacitors C_2 and C_3 are releasing their energy to L_3. A reduced voltage is seen across C_2 and C_4, andV_{in} will provide L_1 with its input voltage.

Applying Kirchhoff's voltage law (KVL) we have

$$V_{L1} = V_{DC} + V_{C1} - V_{C2} \ , \tag{1}$$

$$V_{L2} = V_{C1} \ , \tag{2}$$

and

$$V_{L3} = V_{C2} + V_{C3} \ . \tag{3}$$

Applying Kirchhoff's current law (KCL) we obtain

$$I_{C1} = -2I_{L1} + 2I_{pn} - I_{L3} \ , \tag{4}$$

$$I_{C2} = I_{L1} - I_{pn} \ , \tag{5}$$

$$I_{C3} = -I_{L3} \ , \tag{6}$$

and

$$I_{C4} = I_{L3} - I_{pn} \ . \tag{7}$$

2.2. Non-shoot-through State

Figure 3(b) represents the non-shoot-through state that occurs when the VSI is in operation. Diodes D_2 and D_3 are in reverse-biased condition and are in the OFF state, whereas diodes D_1 and D_4 are in forward-biased condition and are in the ON state. The conduction of D_4 lets the inductors L_1, L_2, L_3, and capacitor C_1, along with V_{in}, discharge the stored energy to the load, while C_3 and C_4 receive from it.

Applying KVL we get

$$V_{L1} = V_{dc} - V_{C2} \ , \tag{8}$$

$$V_{L2} = -V_{C3} \ , \tag{9}$$

$$V_{L3} = -V_{C4} \ , \tag{10}$$

and

$$V_O = V_{C1} + V_{C2} + V_{C3} + V_{C4} \ . \tag{11}$$

Applying KCL we have

$$I_{C2} = I_{L1} - I_{pn} \ , \tag{12}$$

$$I_{C1} = -I_{pn} \ , \tag{13}$$

$$I_{C3} = -I_{pn} + I_{L2} \ , \tag{14}$$

and

$$I_{C4} = I_{L3} - I_{pn} \ . \tag{15}$$

By solving Equations 1-3 and Equations 8-10, we can obtain the voltage across the capacitors as

$$V_{C1} = \frac{D-1}{3D - D^2 - 1} V_{DC} \ , \tag{16}$$

$$V_{C2} = \frac{2D-1}{3D - D^2 - 1} V_{Dc} \ , \tag{17}$$

and

$$V_{C3} = V_{C4} = \frac{D-1}{3D - D^2 - 1} V_{Dc} \ . \tag{18}$$

Under steady-state conditions, an inductor's average voltage throughout a switching period is equal to zero. Consequently, the voltage gain can be determined by applying volt-second balance to the inductors for the proposed topology. From Equation 11, the DC-link voltage can be expressed as

$$V_O = \frac{D-2}{3D-D^2-1} V_{DC} \ . \tag{19}$$

The voltage gain can be obtained as

$$G = \frac{V_O}{V_{DC}} = \frac{D-2}{3D-D^2-1} \ , \tag{20}$$

where D is the duty cycle.

3. Component Parameter Design

To design the proposed topology's inductor, the maximum permissible ripple of the inductor currents must be taken into account. By assuming $K_i\%$ as the ripple of inductor currents, the required inductances can be calculated based on

$$L = \frac{V_L DT}{K_i\% I_L} \ , \tag{21}$$

where V_L is the voltage across the inductor during the shoot-through state and T is the switching period.

Substituting the values into equation 9, the following expressions can be employed for designing the inductors:

$$L_1 = \frac{D(1-D)^2}{2-D} G L_B \ , \tag{22}$$

$$L_2 = DGL_B \ , \tag{23}$$

and

$$L_3 = D(1-D)GL_B \ , \tag{24}$$

and the term L_B in the above equation is defined as

$$L_B = \frac{V_{in}^2}{K_V\% V_C} \ . \tag{25}$$

To design the capacitances for the proposed topology, the maximum voltage ripple generated by the capacitor, denoted $K_V\%$, can be used. This parameter is incorporated in the following equation:

$$C = \frac{I_C DT}{K_V\% V_C} \ , \tag{26}$$

where I_C is the current flowing through the capacitors during the ST state. Hence, the required capacitances can be obtained by the equations

$$C_1 = (1-D)\frac{C_B}{G} \ , \tag{27}$$

$$C_2 = \frac{1-D}{1-3D+D^2}\frac{C_B}{G} \ . \tag{28}$$

$$C_3 = \frac{D}{1-D}\frac{C_B}{G} \ , \tag{29}$$

and

$$C_4 = \frac{1 + D - D^2}{D(2 - D)} \frac{C_B}{G} \ , \tag{30}$$

where C_B is

$$C_B = \frac{PT}{K_V \% V_{in}^2} \ , \tag{31}$$

and P is the nominal power of the converter.

The maximum stored energy depends on the size of the inductors and capacitors, as expressed in the following equations:

$$W_L = \frac{1}{2} L I_{\max}^2, \tag{32}$$

and

$$W_C = \frac{1}{2} C V_{\max} \ . \tag{33}$$

Table 1 compares the proposed topology with conventional topologies such as EB-qZSIs [13], EUG-ASqZSI [7], and ESC-qZSI [9]. It is concluded that the proposed topology uses the same number of elements as the ESC-qZSI proposed in [9] and requires fewer components compared to the EB-qZSIs presented in [13] and EUG-ASqZSI in [7]. Therefore, the proposed concept can be designed at a lower cost.

Table 1. Comparison of component numbers in proposed and conventional topologies.

Components	EB-qZSI [13]	EUG-ASqZSI [7]	ESC-qZSI [9]	Proposed topology
Diodes	5	7	4	4
Inductors	4	3	3	3
Capacitors	4	4	4	4
Switches	6	7	6	6

Table 2 provides the voltage across the capacitors and diodes as well as the current stress of diodes and inductors of the proposed topology.

Table 2. Stresses of the proposed topology.

Parameter	Stress	Parameter	Stress
C_1	$\frac{D-1}{3D-D^2-1} V_{in}$	D_3	$\frac{1}{3D-D^2-1} V_{in}$
C_2	$\frac{2D-1}{3D-D^2-1} V_{in}$	D_4	$\frac{2D-1}{3D-D^2-1} V_{in}$
C_3, C_4	$\frac{D}{3D-D^2-1} V_{in}$	L_1, L_3	$\frac{1+2D}{1-D} Ipn(n)$
D_1	$\frac{D-1}{3D-D^2-1} V_{in}$	L_2	$\frac{1+2D}{1-D} Ipn(n)$
D_2	$\frac{D-1}{3D-D^2-1} V_{in}$		

4. Simulations and Results

The proposed topology is verified by the simulation using MATLAB/Simulink. The parameters for the proposed network were selected as $L_1 = 0.35$ mH, $L_2 = 0.89$ mH, $L_3 = 0.76$ mH, $C_1 = 17$ mF,

$C_2 = 29$ mF, $C_3 = 3.3$ mF, $C_4 = 84$ mF, $f_s = 20$ kHz. These values were obtained from the design equations. Additional parameters, like input voltage and load parameters, are detailed in Table 3.

Table 3. Simulated parameters and values.

Parameter	Values
Rated power, P_o [W]	240W
Input Voltage, V_{dc} [V]	50 V
Output Voltage, V_o [V]	157 V
Switching frequency, fsw [KHz]	20kHz
Inductances (L_1, L_2, L_3) [mH]	0.35, 0.89, 0.76
Capacitances (C_1, C_2, C_3, C_4) [μF]	17.12, 29.07, 3.3, 84

For a 50 V input voltage, the inverter operates with a modulation index M of 0.856 and a duty ratio D of 0.144, which results in a voltage gain of three times compared to the input voltage. The theoretical output voltage is determined to be 157 V, while the simulated value is 153 V, as shown in Figure 4. This figure represents the simulation results of the input voltage and capacitor voltages of the proposed topology. The first lane represents the input voltage, while the subsequent lanes represent the capacitor voltages. The voltages of capacitors C_1 and C_2 are boosted to $V_{C1} = 70$ V and $V_{C2} = 59$ V respectively, while voltages of C_3 and C_4 are bucked to $V_{C3} = 11$ V and $V_{C4} = 10$ V. This process is continuous for every cycle.

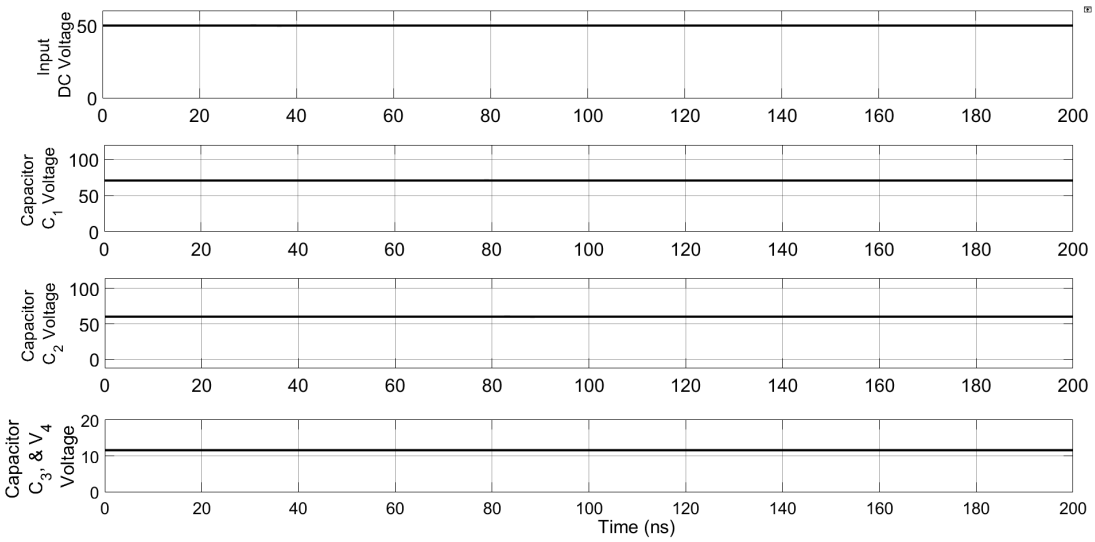

Figure 4. Simulation results of input voltage and capacitor voltages of the proposed topology.

Figure 5 represents the simulation results of the DC-link voltage and inductor currents in the proposed topology. The first lane represents the DC-link voltage with V_{pn} of 153 V, while the other three lanes showcase the inductor currents and the current waveforms of the inductors L_1, L_2, and L_3 with values $I_{L1} = 3.36$ A, $I_{L2} = 1.75$ A, $I_{L3} = 3.49$ A. When the inverter bridge legs are shorted, the inductor stores energy in the form of an electromagnetic field. As a result waveform is raised during the ST period. During the NST period the inductor releases the energy, causing the waveform to fall. This process is continuous for every cycle.

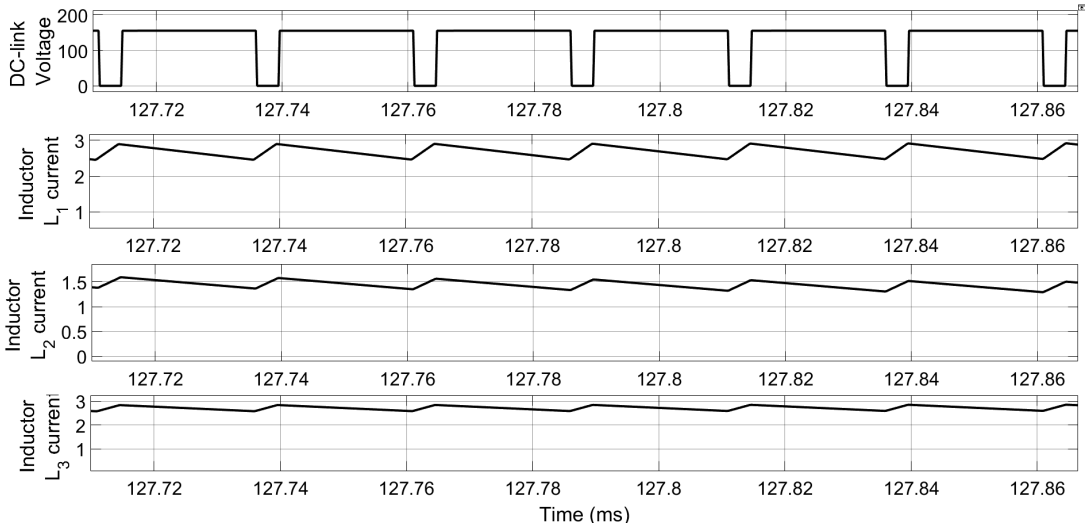

Figure 5. Simulation results of DC-link voltage and currents in inductors L_1, L_2 , and L_3 of the proposed topology.

Figure 6 represents the simulation results of inductor voltages in the proposed topology. The first line showcases the voltage across the inductor L_1, while the other lines represent the voltage across inductors L_2 and L_3. During the ST state, the inductors store energy and release it during the NST state. The voltage values of the inductors are $V_{L1} = 10$ V, $V_{L2} = 11$ V, and $V_{L3} = 10.7$ V, as shown in Figure 6.

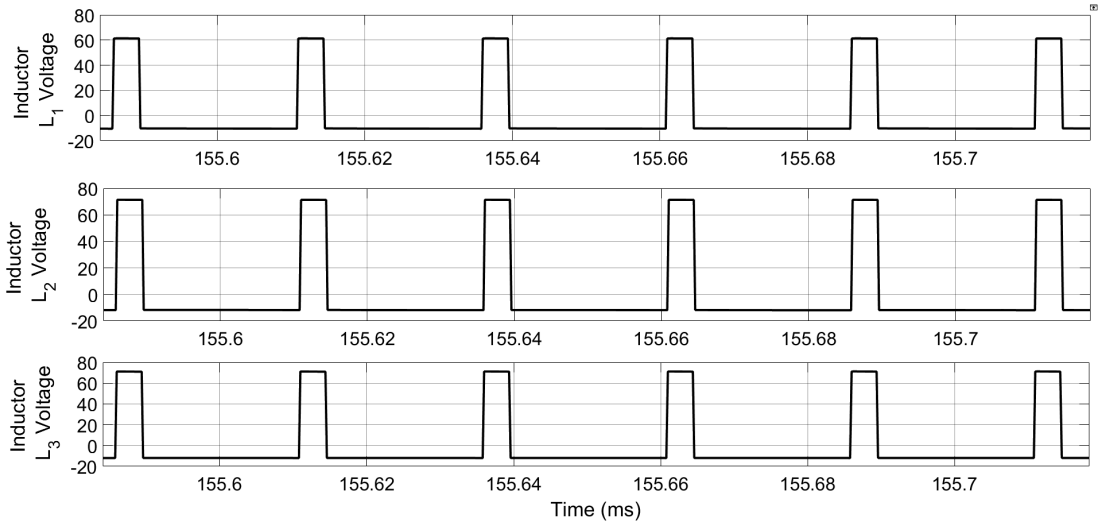

Figure 6. Simulation results of inductor voltages of the proposed topology.

Figure 7 represents the simulation results of the diode voltages of the proposed topology, i.e., voltage stresses across diodes D_1, D_2, D_3, and D_4 with values of $V_{D1} = 69$ V, $V_{D2} = 73$ V, $V_{D3} = 83$ V and $V_{D4} = 80$ V. The figure shows that when the converter is in the ST state, diodes D_2 and D_3 are forward-biased (conducting), and the voltage across the diodes is ideally zero. In the meantime, D_1 and D_4 are reverse-biased and block the voltage. Conversely, in the NST state, diodes D_1 and D_4 are forward-biased (conducting), and the voltage across the diodes is ideally zero, while D_2 and D_3 are reverse-biased and block the voltage.

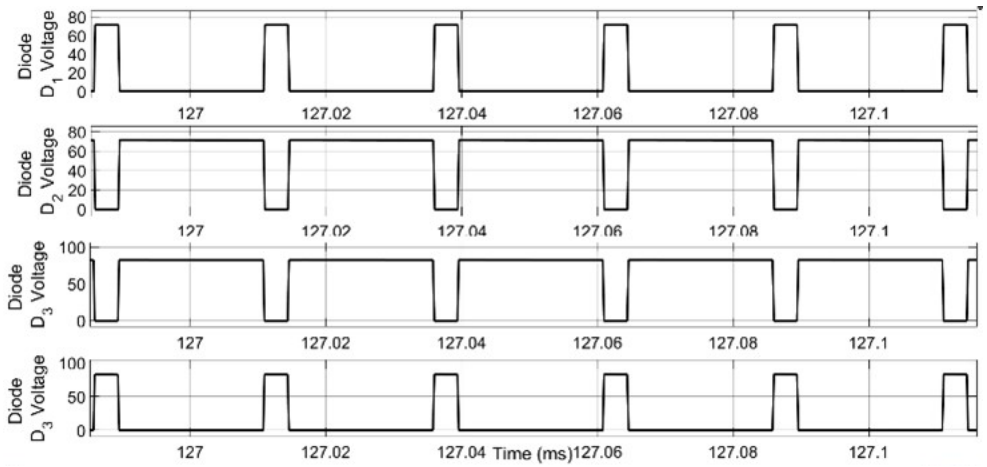

Figure 7. Simulation results of diode voltages of the proposed topology.

Figure 8 illustrates the simulation results of diode currents. In the non-shoot-through state, diodes D_1 and D_4 are in the ON state, conducting current. Conversely, in the shoot-through state, these diodes are in the OFF state due to reverse-biased conditions. Therefore, during this state, no current flows through these diodes.

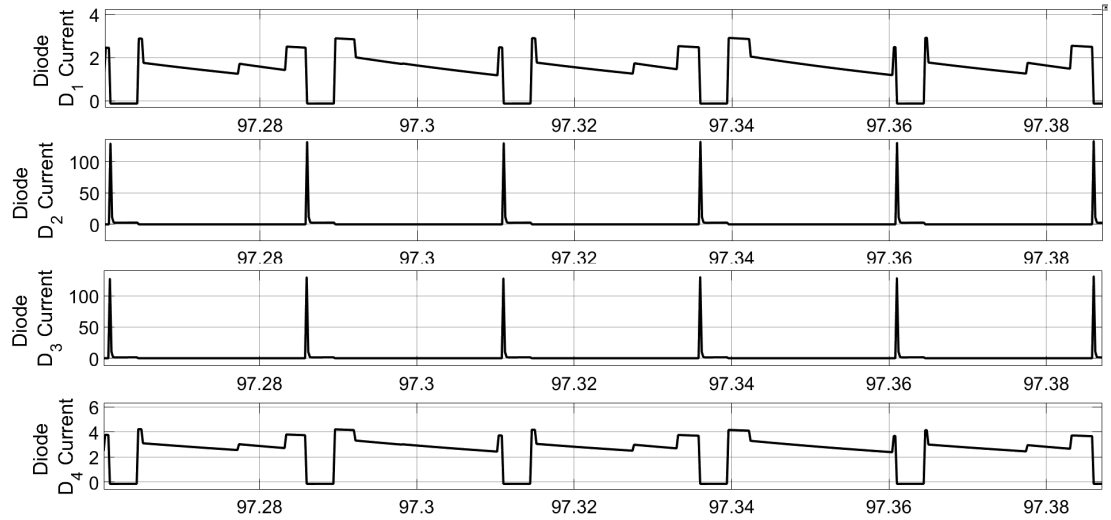

Figure 8. Simulation results of diode currents of the proposed topology.

Figure 9 represents the outputs of the inverter. The first lane represents the phase-A voltage of the inverter bridge. The line voltage acquired using Simulink is 102 V. The phase voltage of the inverter measured was 63 V. The output current flowing through the load is approximately 1.23 A. The output voltage is of a square nature due to the absence of a filter, but the output current is sinusoidal in nature due to the presence of load inductance. This illustrates the impact of filtering components and load on the outputs of an inverter.

Connecting the L-C filter across the load minimizes ripples at the output, resulting in ripple-free waveforms or sinusoidal waves across the load, as depicted in Figure 10.

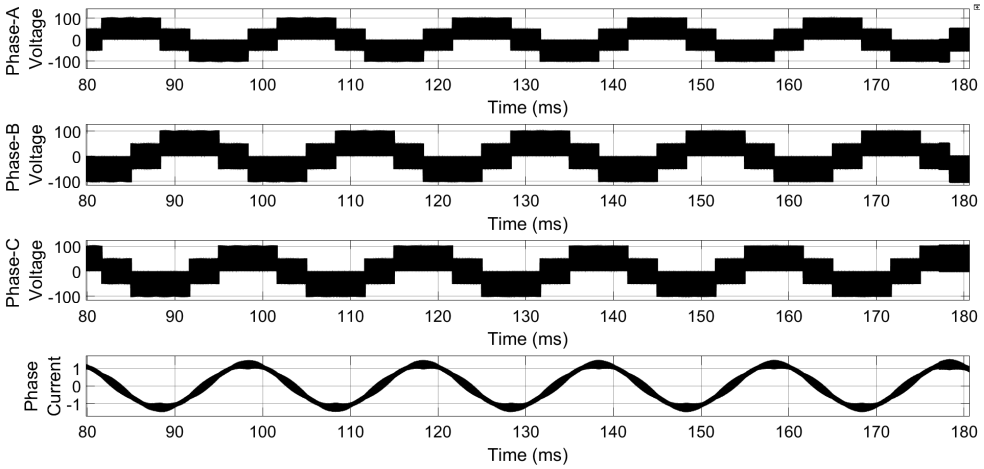

Figure 9. Simulation results of inverter output phase voltages and output current of the proposed topology without filter.

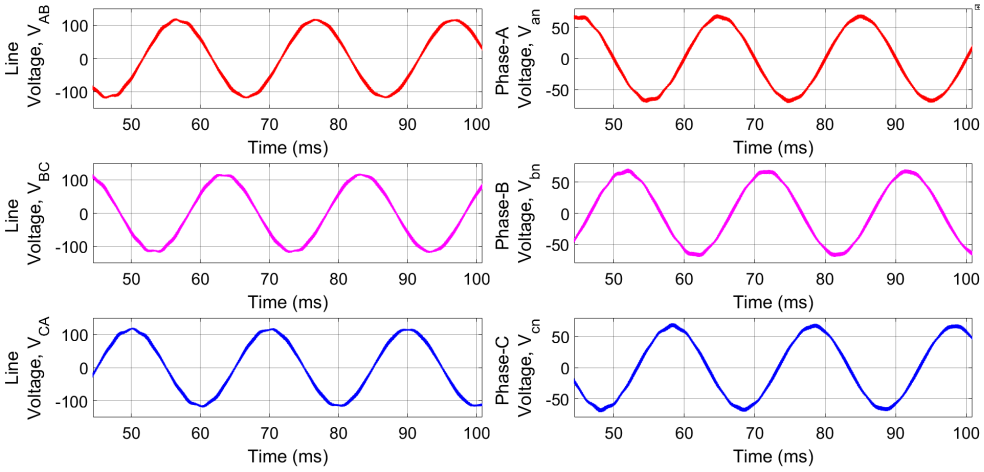

Figure 10. Simulation results of line and phase output voltages with filter.

5. Conclusions

One of the main advantages of the capacitor-switched type Z-source inverter is its ability to reduce the voltage stress on the switches. This results in lower switching losses, which improves efficiency and reduces the thermal stress on the components. The use of capacitors also allows for faster and smoother current control, which enhances the stability and reliability of the inverter.

However, there are some challenges that need to be addressed in the capacitor-switched type Z-source inverter technology. One of the challenges is the selection and size of the capacitors, which can affect the overall efficiency and performance of the inverter. The switching frequency also needs to be carefully controlled to minimize the losses and optimize the performance of the inverter.

In conclusion, the capacitor-switched type Z-source inverter is a promising technology that offers many advantages over traditional inverters. Further research and development are needed to fully explore the potential of this technology and to address the challenges associated with it. With continued improvements and innovations, the capacitor-switched type Z-source inverter has the potential to become a key player in the field of power electronics.

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