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Article

Boundary-Based PWM Control Scheme for a DC-DC Buck Converter Operating in CCM

Hardik Patel[1,†], **Ankit Shah**[2,*]

[1] Instrumentation and Control Engineering Department, Government Engineering College, Rajkot, Gujarat Technological University, India.

[2] Instrumentation and Control Engineering Department, L. D. College of Engineering, Gujarat Technological University, Ahmedabad, India.

[†] PhD Research Scholar, Gujarat Technological University, Ahmedabad, India.

[*] Correspondence: ankitshah.ic@ldce.ac.in

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Abstract: This paper presents a control scheme for DC-DC buck converters operating in Continuous Conduction Mode (CCM) that achieves fast and accurate regulation of the output voltage while reducing the computational burden on the control system. The study investigates the boundary-based control scheme for a buck converter and models the converter circuit as a Switched Dynamical System (SDS) using hybrid automaton due to its continuous and discrete states. The boundaries of these states are determined to enable the implementation of a fixed-frequency Pulse-Width Modulation (PWM) control scheme. The proposed control scheme was evaluated through simulation with variations in input voltage, load, and reference voltage. It was further analyzed for model mismatch due to parametric variations and parasitic parameters, which demonstrated its effectiveness and robustness under various operating conditions. The SDS approach for controlling the buck converter is simple, requires minimal mathematical calculations, and is free from modeling errors. The output voltage was stable under regulatory and servo problems, as well as sinusoidal input testing. The proposed scheme was compared with other conventional schemes and found superior in terms of steady-state and dynamic response. Additionally, integral compensation was introduced to counter parasitic parameters, which was found to be effective.

1. Introduction

DC-DC converters have become an essential component in many electronic systems due to their ability to efficiently convert a DC voltage from one level to another while maintaining a stable output voltage. This makes them ideal for use in a wide range of applications, including automobiles, telecommunications devices, medical devices, renewable energy systems, and many more [1]. Among the various topologies of

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DC-DC converters, the buck converter is one of the most commonly used topologies for step-down power conversion. However, the presence of switching elements in the circuit makes the controller design more complicated.

Among the recent research in the field of DC-DC converters, both small-signal and large-signal models are commonly used to study the behavior of the system under different operating conditions [2, 3, 4]. Small-signal models derived using state-space analysis are useful for designing control systems and analyzing the stability and performance of the converter. The drawback of small-signal models is that they assume dynamics slower than the switching frequency, which can lead to inaccurate predictions of the system behavior and suboptimal control design [5]. Small signal models are more suitable for linear analysis, while large signal models can capture non-linear behavior but are computationally more demanding and require accurate model information. Both methods have robustness and sensitivity issues that can be mitigated with proper modeling and control design techniques [5].

It is often recommended to use conventional controllers, such as Proportional Integral Derivative (PID), for controlling the output voltage of buck converters [6]. Modified PID algorithms have been proposed to improve the performance of the controller [7, 8]. However, tuning such controllers requires a rigorous trial-and-error process.

Boundary Control (BC) is a control strategy that has garnered attention for its geometric-based approach to regulating the performance of DC-DC converters. Analog circuits have traditionally been the primary choice for implementing BC. However, there is a growing trend toward digital control [9]. But, due to the need for high sampling rates and processor speeds to obtain instantaneous voltage and current measurements, the practical implementation of BC in high-frequency DC-DC converters is constrained [10]. It is important to consider the issue of robustness when it comes to DC-DC converters using BC. Geometric controls have the potential to offer faster dynamic responses, but simple linear boundary-based solutions are rarely optimal [5]. Non-ideal factors such as parametric variations and parasitic parameters can significantly impact the large-signal behavior of the system, which is not often addressed [11]. Moreover, all these control approaches require a large number of mathematical calculations.

Studies and presentations of control techniques for DC-DC converters in the form of SDS and hybrid systems have been focal points for researchers. Mirzaei and Afzalian [12] designed an explicit model predictive controller using current-mode control to regulate the inductor current of a buck-boost converter based on a set of non-linear equations. However, this model required complex and computationally intensive controller design. A case study on embedding hybrid automata into integrated model-based design frameworks for the correct-by-construction compositional design of cyber-physical systems was validated by Bak et al. [13] on a closed-loop buck converter. One of its potential disadvantages is that the translation process is parametrized by an ϵ relaxation, which can result in an under-approximation or over-approximation of hybrid automaton trajectories, depending on the value of ϵ. Zhang et al. [14] presented a switched linear system model for controllability analysis of non-linear high-order dc-dc converters. However, it results in uncontrollability in some cases where state variables have direct relations due to the physical features of the circuit, and it does not extensively model parasitic parameters of electronic components, which may have effects on other converters. Yang et al. [15] proposed a framework for identifying and validating affine hybrid automata from input-output traces. One disadvantage of their method is that it requires input and output traces to learn the hybrid automata, which may not always be available or easily obtainable. Additionally, the framework relies on the accuracy of the ordinary differential equation estimations and the clustering method used for the segmentation of traces, which may not always be perfect, leading to potential errors in the resulting automaton. Still, all these approaches are complex and require significant mathematical computation.

To address the issues mentioned above, we propose a boundary-based PWM approach with minimal mathematical computations. In this approach, the buck converter is modeled as SDS, and parasitic parameters are counteracted by integral compensation. As a Current-Mode Control (CMC) technique, it offers superior current regulation compared to Voltage-Mode Control (VMC) which is particularly advantageous for applications with variable loads or high ripple currents. The reason is that CMC directly regulates the current flowing through the inductor, whereas VMC regulates the output voltage by indirectly controlling the inductor current through the error amplifier, which can result in slower response and poor stability under certain conditions. Additionally, CMC can provide inherent protection against over-current conditions, making it a more robust control technique. To assess the efficacy of the proposed method, we carried out circuit-level simulations in MATLAB/SIMULINK. The simulation results show that the proposed control scheme has superior set-point tracking capability and is relatively insensitive to load changes, parametric variations, and parasitic parameters.

2. Methodology

A conventional circuit of the buck converter is shown in Figure 1, while Table 1 displays the notation used for analysis. Although all components are assumed to be ideal for analysis, the compensation mechanism of parasitic values is taken into account.

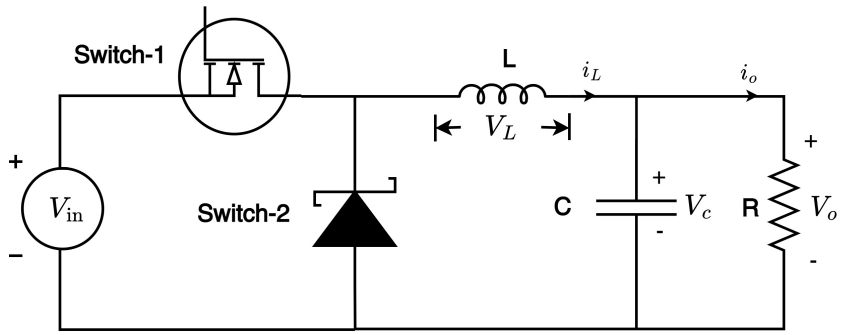


Figure 1. The circuit diagram of a conventional buck converter.

Symbol	Description	Symbol	Description
Switch-1	MOSFET	Δi_L	Ripple in inductor current
Switch-2	Diode	I_{UP}	Upper peak value of i_L
f	Switching frequency of MOSFET	I_{LP}	Lower peak value of i_L
D	Duty cycle	V_C	Average voltage across capacitor
V_{in}	Input voltage	v_o	Instantaneous output voltage
V_{ref}	Reference or Set-point voltage	V_o	Average output voltage
V_L	Voltage across inductor	Δv_o	Output voltage swing
i_L	Instantaneous inductor current	M_p	Peak overshoot
I_L	Average value of inductor current	T_s	Settling time

Table 1. Notation for analysis of buck converter circuits.

2.1. State-space modeling

Let $X \in R^n$ be continuous state and k takes values in finite set $K = \{1, ..., N\}$ and is discrete state. represents the on/off configuration of MOSFET and diode. For each $k \in K$, continuous dynamics is modeled by the differential equation

$$\dot{x}(t) = A_k x(t) + B_k \ , \tag{1}$$

where $x \in X$ is the state vector, $A_k \in R^{n\times n}$ is the system matrix and $B_k \in R^{n\times 1}$.

The presence of two switches in the circuit enables the possibility of discrete states. Therefore, the second-order switched buck converter has four discrete states. Each of them corresponds to a specific state matrix, as detailed in Table 2. Figure 2 illustrates the circuit diagram for states k_1 and k_2. State k_3 belongs to discontinuous conduction mode, and k_4 is not feasible. Therefore, the circuits for those states are not shown.

Operating mode (K_i)	Switch-1	Switch-2	A_i	B_i
k_1	ON	OFF	$\begin{bmatrix} 0 & -1/L \\ 1/C & -1/RC \end{bmatrix}$	$\begin{bmatrix} V_{in}/L \\ 0 \end{bmatrix}$
k_2	OFF	ON	$\begin{bmatrix} 0 & -1/L \\ 1/C & -1/RC \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$
k_3	OFF	OFF	$\begin{bmatrix} 0 & 0 \\ 0 & -1/RC \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$
k_4	ON	ON	Impractical	

Table 2. Possible discrete state and corresponding system state matrices.

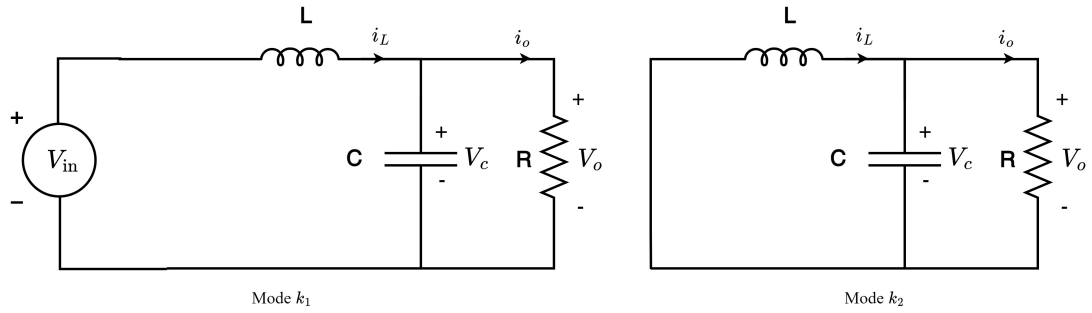


Figure 2. Buck converter during different modes.

2.2. Buck converter as SDS

The SDS is a special class of hybrid system and mathematically it can be described by [16, 17]

$$\dot{x}(t) = f_\sigma(x(t), u(t)) \ , \tag{2}$$

where $x(t)$ is the state of the system at time t, $u(t)$ is the control input at time t, $\dot{x}(t) = f_\sigma(x(t), u(t))$ is the state-transition function, which describes the dynamics of the system in the σ mode of operation. The operation of the system is determined by a switching signal σ that is defined by a set of state-dependent boundaries.

The buck converter is modeled as SDS with two modes:

1. During the ON time of the MOSFET, the dynamics of the system are described by a Linear Time-Invariant (LTI) system where the input voltage is applied to the inductor and the output voltage is regulated by the switching action of the diode.
2. During the OFF time of the MOSFET, the dynamics of the system are described by a different LTI system where the inductor discharges through the output capacitor, resulting in a voltage drop.

The switching between these two modes is governed by the D of the MOSFET, which determines the amount of time the switch spends in each of them.

The operation of the buck converter, which consists of passive components and switches, can be effectively captured through a hybrid automaton. Figure 3 demonstrates the representation of the buck converter circuit as a hybrid automaton. This hybrid automaton can be defined by tuple $H = \{K, X, I, E, F, g, J\}$ which has the following components [13]:

- K : The finite set of modes corresponds to the discrete states of the buck converter. In the case of the second-order switched buck converter, there are four possible modes, each corresponding to a specific combination of switch states.
- X : The finite-dimensional continuous state space represents the continuous variables of the buck converter. This includes current flowing through the inductor and voltage across the capacitor.
- I : The finite set of inputs represents the exogenous signals that influence the dynamics of the buck converter, which includes the input voltage.
- E : The finite set of disturbances represents the uncertainties or perturbations in the system, such as noise or fluctuations in the input voltage.
- F : The set of flow functions describes the continuous dynamics of the system within each mode. For the buck converter, these flow functions describe the behavior of the inductor and capacitor as well as the switches during each mode of operation.
- g : The set of guard conditions specifies the conditions under which a mode transition can occur. For the buck converter, these guard conditions correspond to the boundaries that define when the system switches to a new mode of operation.
- J : The set of jump maps describes the discrete dynamics of the system during a mode transition. For the buck converter, these jump maps describe the change in state variables that occurs when the system switches to a new mode of operation.

3. Controller Design

In the context of the SDS framework, the control problem of a buck converter is simplified as the selection of jump maps (J) such that a constant frequency PWM scheme is characterized. For closed-loop control, the continuous and discrete transitions of the buck converter are controlled by boundary conditions set by J. The continuous transitions are controlled by boundary conditions set up by inductor current and output voltage, while discrete transitions are controlled by turning ON and OFF the MOSFET. When the continuous-time variable exceeds the boundary conditions set by J, the discrete transition is triggered.

In CCM operation of a buck converter, J_{12} and J_{21} , which represent the transition between the continuous and discrete modes, are considered as J. The approximation of inductor current and output voltage waveforms in Figure 4 refers to the CCM operation of a buck converter. In CCM, the inductor current never reaches zero, and the current and voltage waveforms have a continuous ripple.

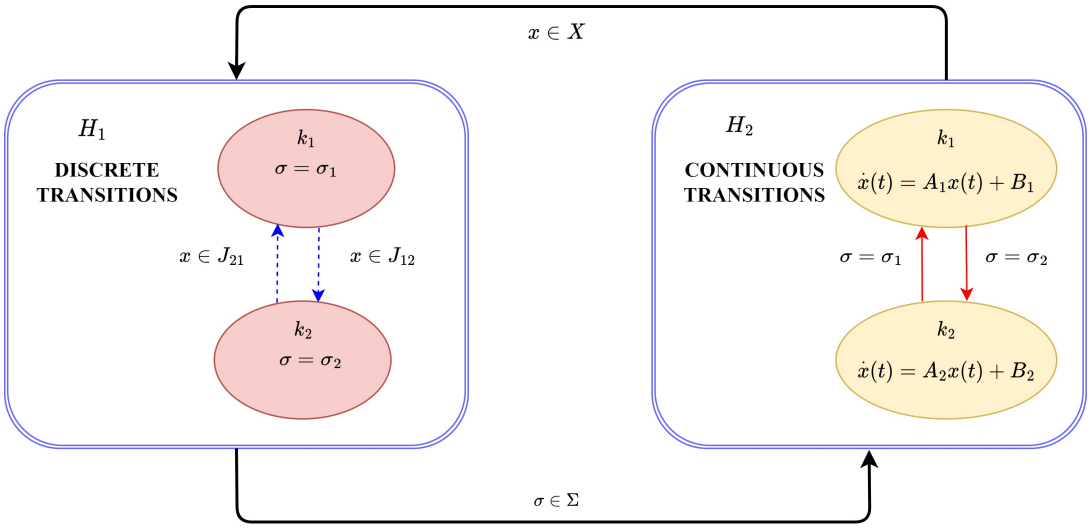


Figure 3. Hybrid automaton representation of switched buck converter shown as an interaction of continuous and discrete transitions.

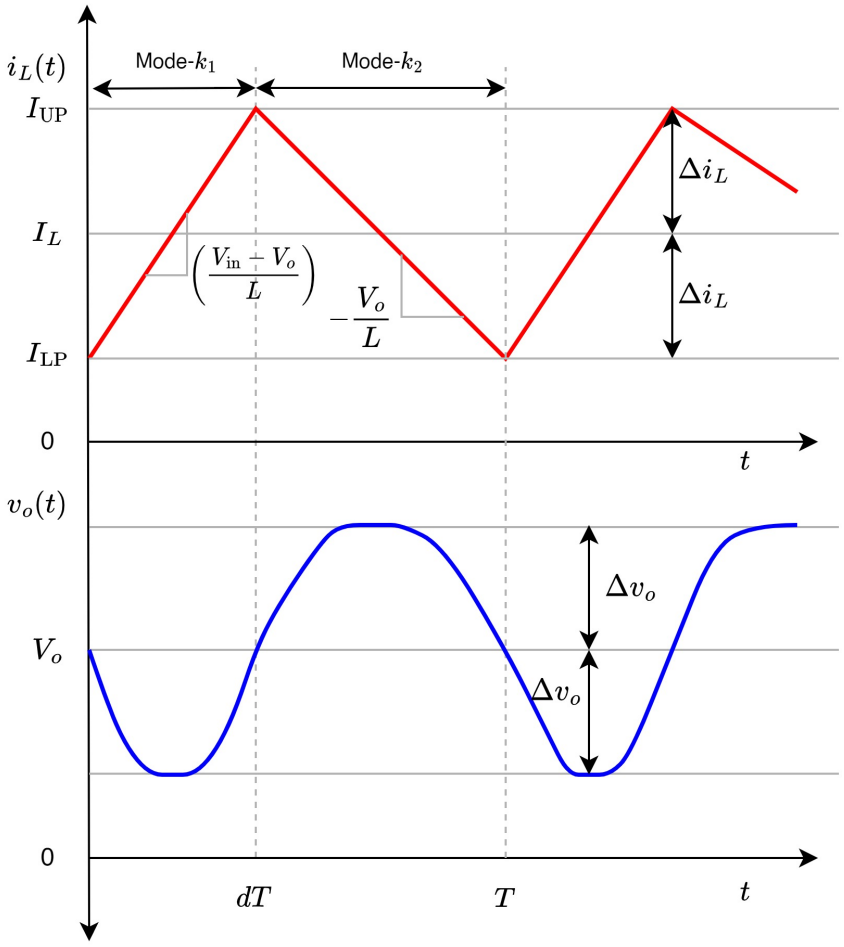


Figure 4. Approximated waveforms of state variables of buck converter in CCM.

The voltage across the inductor, when MOSFET is ON, can be calculated as

$$V_{L(ON)} = -(V_{in} - V_o) \ . \tag{3}$$

The inductor voltage during the OFF state of MOSFET can be calculated by

$$V_{L(OFF)} = V_o \ . \tag{4}$$

In steady-state, the average inductor current in a cycle is zero and that can be expressed by

$$V_{L(ON)}dT + V_{L(OFF)}(1-d)T = 0 \ . \tag{5}$$

Substituting equation (3) and (4) in equation (5), and solving for d, we get

$$d = \frac{V_o}{V_{in}} \ , \tag{6}$$

where d is the voltage ratio.

The change in inductor current can be calculated as

$$2\Delta i_L = I_{UP} - I_{LP} = \frac{V_{in} - V_o}{L} dT \ . \tag{7}$$

Substituting equation (6) in (7) we get

$$\Delta i_L = \frac{V_o(V_{in} - V_o)}{2Lf V_{in}} \ , \tag{8}$$

where $f = 1/T$ and T is the time period.

The average inductor current for buck converter in CCM is

$$I_L = \frac{V_o}{R} \ . \tag{9}$$

Finally, the J is defined as

$$J_{12} : i_L \geq I_{UP} \Rightarrow i_L \geq I_L + \Delta i_L \ . \tag{10}$$

Similarly, the J_{12} is given by

$$J_{21} : t \geq T \ . \tag{11}$$

According to equation (8), Δi_L and f are inversely proportional, which means that a careful selection of the switching frequency is necessary to avoid switching losses. Figure 5 displays the block diagram of the closed-loop control scheme, incorporating integral compensation to address parasitic values. Further detail regarding the integral compensation technique is analyzed in the result and discussion section.

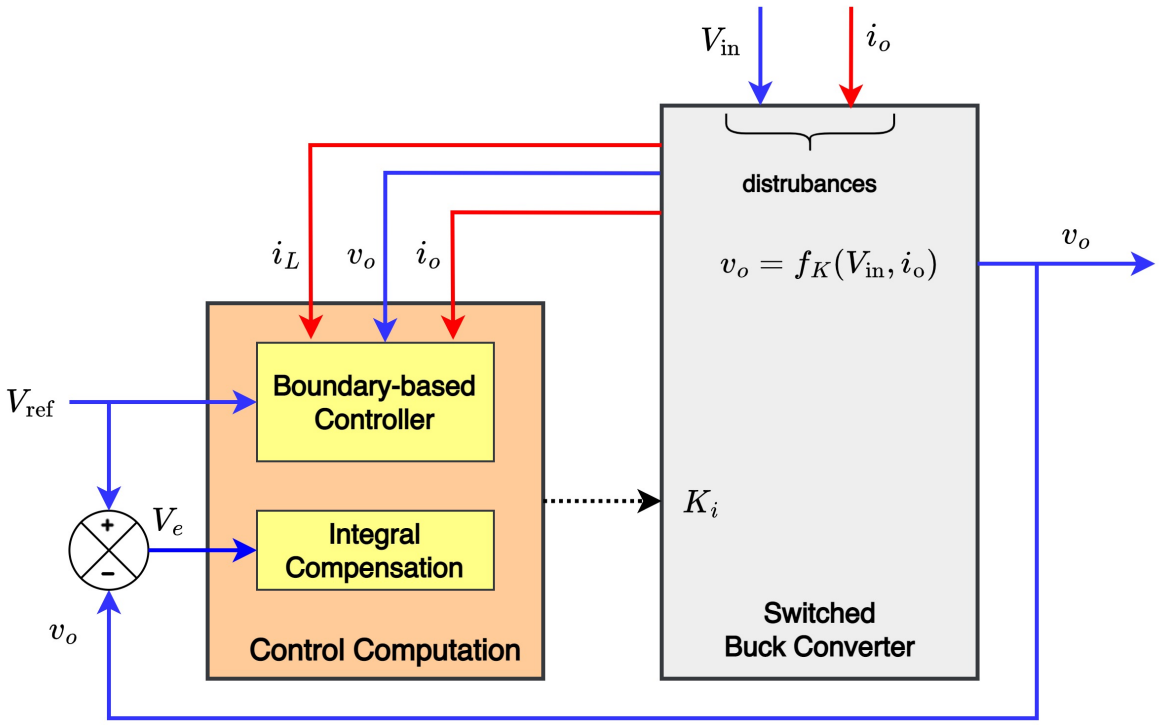


Figure 5. The complete closed-loop control diagram of the proposed scheme.

4. Results and Discussion

The proposed control scheme was simulated using MATLAB/SIMULINK version R2020b, with the buck converter parameters shown in Table 3. The control scheme proposed in the study is illustrated through a simulation diagram in Figure 6. The diagram depicts the interconnection of various MATLAB/SIMULINK blocks that are utilized to implement the control scheme, with specific processes highlighted and separated to ensure clarity in the overall design. Figure 7 presents an overview of the simulation results, while Table 4 provides a comprehensive analysis that delves deeper into the findings. The detailed analysis in Table 4 offers valuable insights and allows for a more nuanced interpretation of the simulation results.

Parameter	Nominal value	Parasitic value
L - Inductor	$550\mu H$	$r_L - 150m\Omega$
C - Capacitor	$10\mu F$	$r_c - 1\Omega$
R - Load resistor	5Ω	-
MOSFET	-	$R_{DS(ON)} - 3m\Omega$, $V_{SD} - 0.7$ V
Diode	-	$V_d - 0.4$ V
V_{in}	12V	-
V_{ref}	5V	-
f	25kHz	-

Table 3. Parameters of the buck converter.

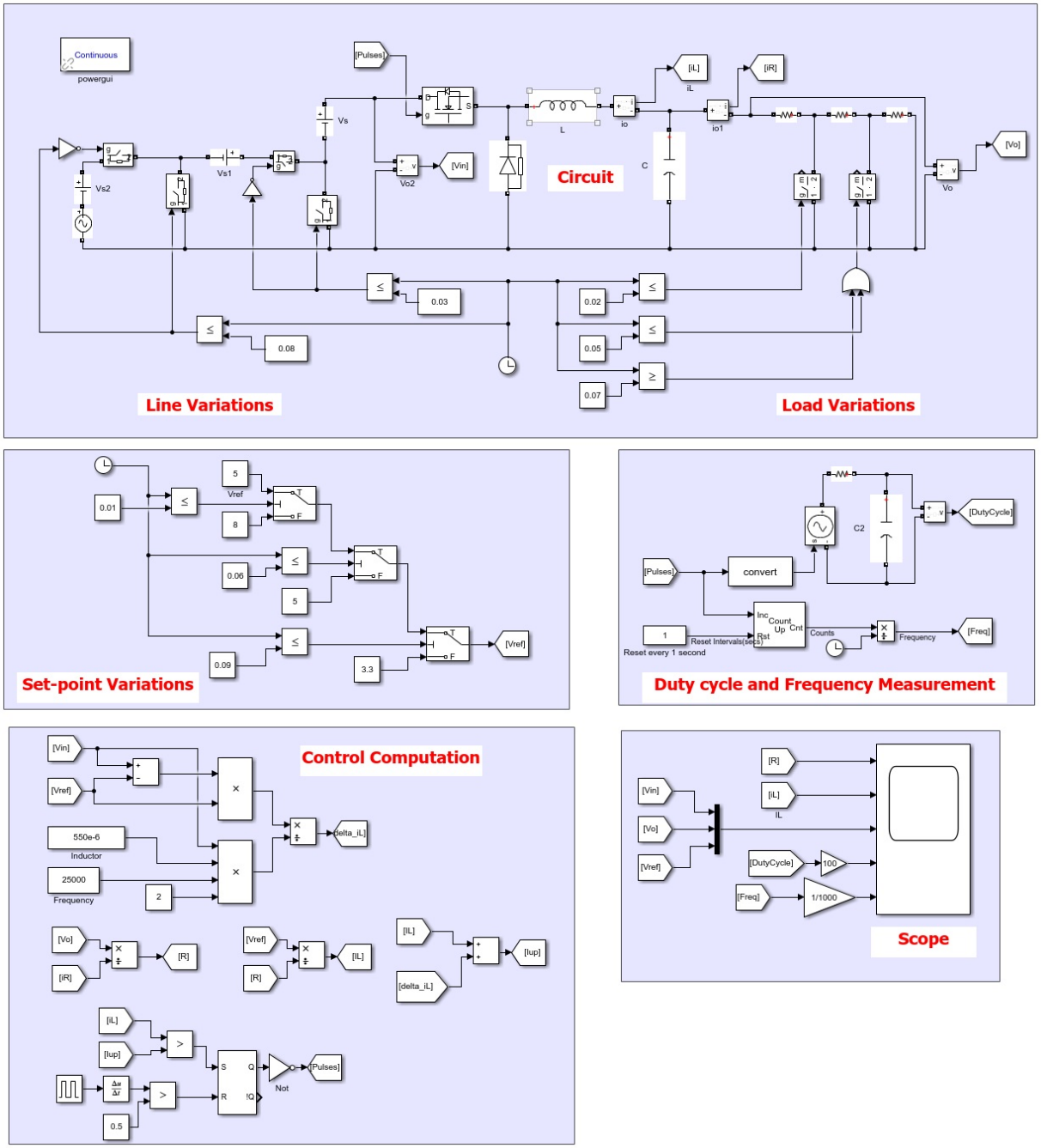


Figure 6. Simulation diagram of boundary-based PWM control scheme for buck converter.

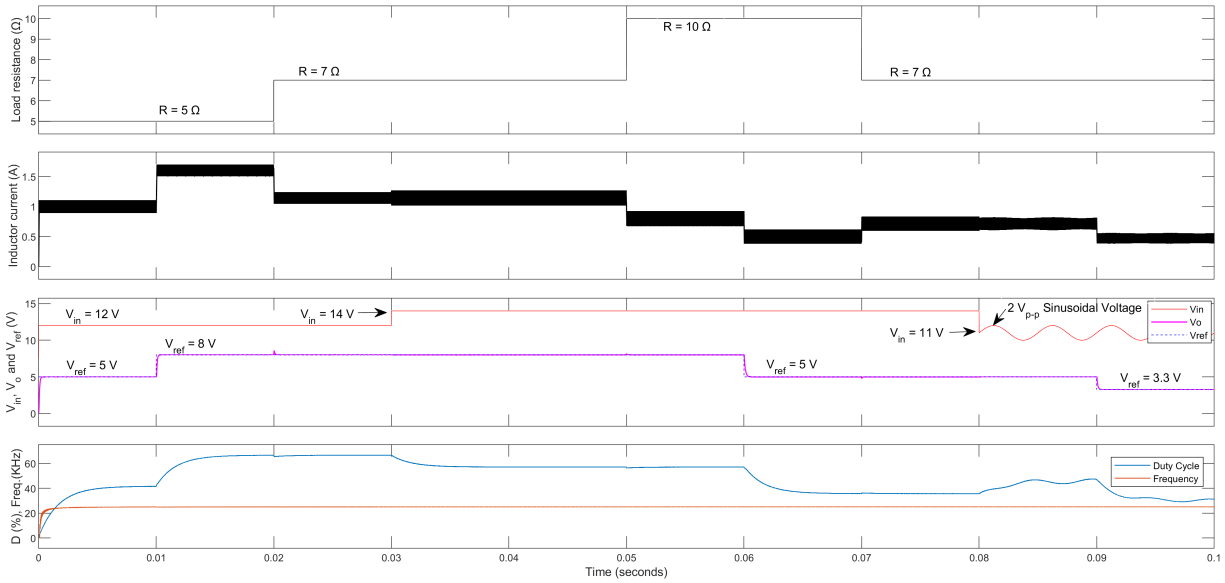


Figure 7. Overall simulation results of the proposed scheme

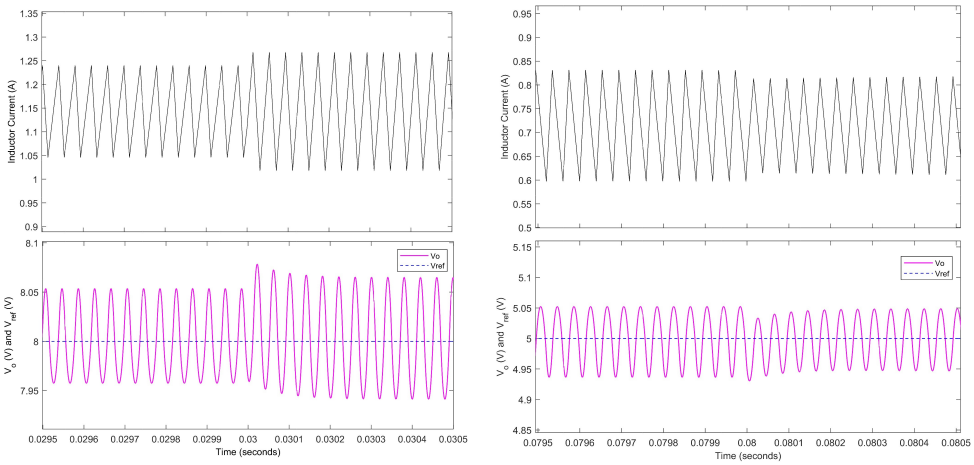
Time Span	R	$V_{in}(V)$		V_{ref}	D	M_p	T_s	Problem
(s)	(Ω)	$V_{DC}(V)$	$V_{AC}(V_{pp})$	(V)	(%)	(%)	(ms)	
[0-0.01)	5	12	-	5	[0-41.5)	1	0.3	-
[0.01-0.02)	5	12	-	5→8	[41.5-66.5)	0.6	0.3	Servo: Set-point
[0.02-0.03)	5→ 7	12	-	8	[65.5-66.6)	7.5	0.3	Regulatory: Load
[0.03-0.05)	7	12→14	-	8	[66.6-57.2)	1	-	Regulatory: Input voltage
[0.05-0.06)	7→10	14	-	8	[56.3-57.2)	2.5	0.4	Regulatory: Load
[0.06-0.07)	10	14	-	8→5	[56.4-36.8)	1.2	0.5	Servo: Set-point
[0.07-0.08)	10→7	14	-	5	[36.2-36.7)	4.8	0.3	Regulatory: Load
[0.08-0.09)	7	14→11	0→2	5	[36.7-47.5)	0	-	Regulatory: Input voltage
[0.0-0.1)	7	11	2	5→3.3	[47.5-31.4)	1.15	0.5	Servo: Set-point

Table 4. Detailed analysis of D, M_p, and T_s during line, load, and set-point variations.

4.1. Response to regulatory and servo problems

4.1.1. Regulatory problem (Input voltage)

The simulation results presented in Figure 8 demonstrate the superior performance of the controller in response to regulatory load problems. Furthermore, the simulation shows that even when the input voltage is lowered to 11 V and a sinusoidal voltage is applied simultaneously at $t = 0.08$ s, the controller can keep the output voltage stable without any overshoot or undershoot. This result indicates the controller's robustness and reliability in regulating the output voltage, even under challenging operating conditions.

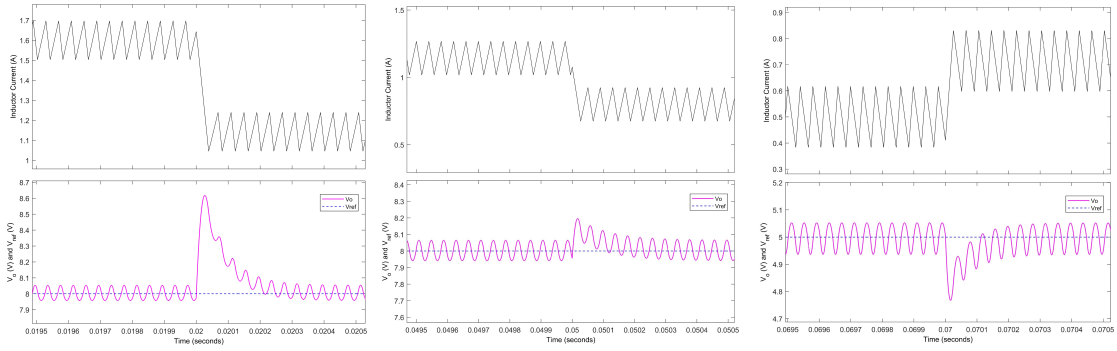


(a) $t = 0.03$ s **(b)** $t = 0.08$ s

Figure 8. State variables transients during line variations: (a) waveforms of i_L and v_o for change in V_{in} from 12 V to 14 V at $t = 0.03$ s. (b) waveforms of i_L and v_o for simultaneous change in V_{in} from 14 V to 11 V and variation of $2V_{pp}$ sinusoidal voltage at $t = 0.08$ s.

4.1.2. Regulatory problem (Load)

Figure 9 depicts the controller's response to various load disturbances, with plots of the inductor current and the output voltage. At $t = 0.02$ s, when the load is increased by 40% and the set-point is 60% higher than the nominal parameter, the system exhibits a maximum overshoot of 7.5%. This result indicates that the controller effectively dampens the system's response to external disturbances, ensuring the output remains within acceptable limits.

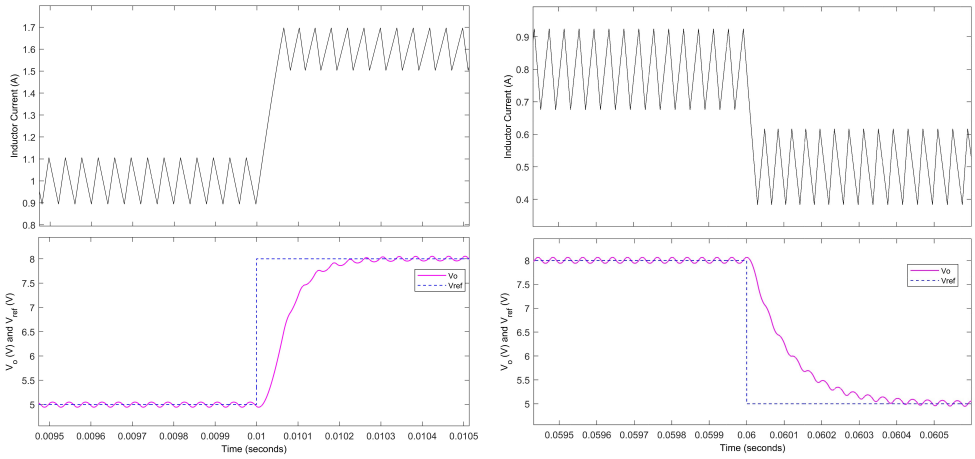


(a) $t = 0.02$ s **(b)** $t = 0.05$ s **(c)** $t = 0.07$ s

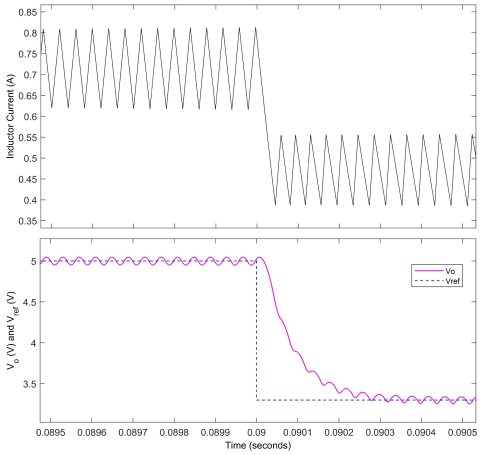
Figure 9. State variables transients during load variations: (a) waveforms of i_L and v_o for change in R from 5Ω to 7Ω at $t = 0.02$ s. (b) waveforms of i_L and v_o for change in R from 7Ω to 10Ω at $t = 0.05$ s. (c) waveforms of i_L and v_o for change in R from 10Ω to 7Ω at $t = 0.07$ s.

4.1.3. Servo problem (Set-point tracking)

The controller's superior performance in addressing servo problems is evidenced by the results in Figure 10, indicating its effectiveness in responding to such problems. The plots clearly show that the controller can quickly and accurately track changes in the set-point, without any overshoot or undershoot. In particular, when the set-point is reduced to 3.3 V with the sinusoidal input voltage, the output voltage still tracks the reference accurately, as shown in Figure 7 and Figure 10c.



(a) $t = 0.01$ s **(b)** $t = 0.06$ s



(c) $t = 0.09$ s

Figure 10. State variables transients for set-point variations: (a) waveforms of i_L and v_o for change in V_{ref} from 5 V to 8 V at $t = 0.01$ s. (b) waveforms of i_L and v_o for change in V_{ref} from 8 V to 5 V at $t = 0.06$ s. (c) waveforms of i_L and v_o for change in V_{ref} from 5 V to 3.3 V at $t = 0.09$ s.

Overall, the simulation results demonstrate the superior performance of the proposed controller for both regulatory and servo control problems, as it maintains stable output voltage without significant overshoot or undershoot.

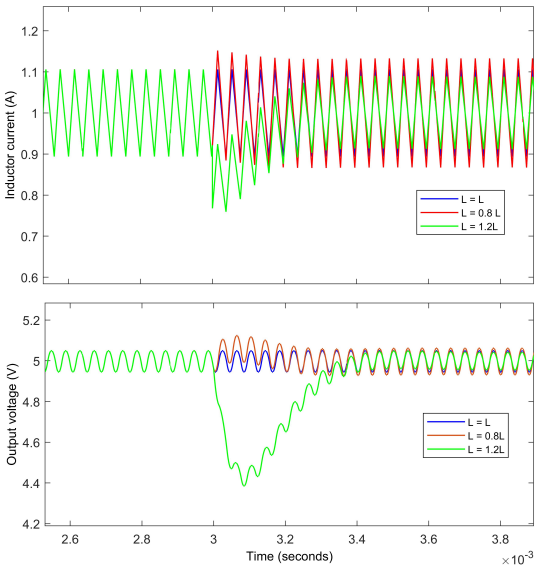
4.2. Analysis of model mismatch

Although the simulation results derive from precise SDS modeling, practical circuits are susceptible to various sources of inaccuracies, such as parametric variations and parasitic parameters. As a result, it is crucial to evaluate the effects of these discrepancies and discuss potential solutions to mitigate their impact on the system's performance.

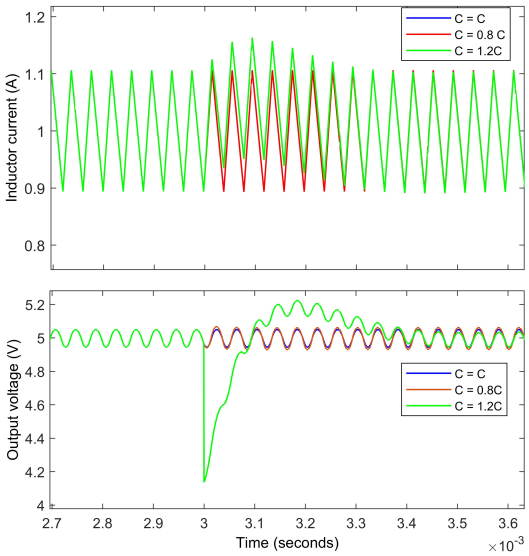
4.2.1. Parametric variations

The inductance value in DC-DC converters can undergo permanent variation due to several factors such as saturation, core material, temperature, mechanical stress, and aging, which ultimately impact the

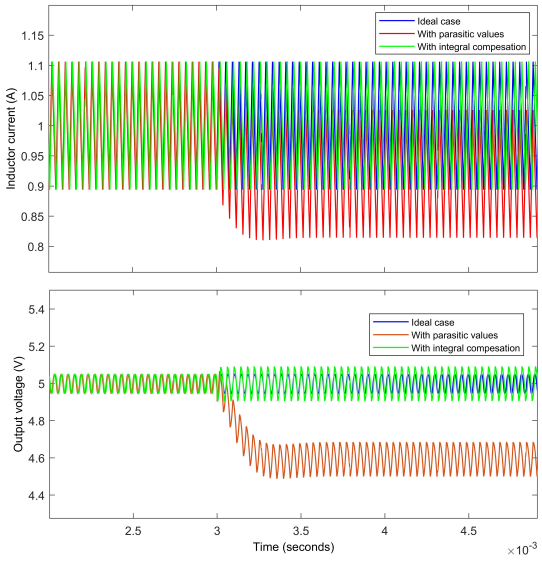
performance of the converter. There is a variation of ±20% in the inductance value is considered, while keeping all other nominal parameters constant. As per equation (8), reducing the inductor value causes an increase in Δi_L, which is reflected in Figure 11a. This is because the inductor will need to store the same amount of energy as before, but with a smaller inductance value, the current must increase to maintain the same energy storage. A slight overshoot in output voltage is visible due to the high Δi_L . Similarly, a higher inductance value results in a smaller Δi_L, as confirmed by Figure 11a. Although there is a visible undershoot, it quickly settles to the setpoint.



(a) ±20% variations in inductance



(b) ±20% variations in capacitance



(c) Parasitic parameters effects

Figure 11. Simulation results for model mismatch analysis: (a) Simulation results with ±20% variations in inductance. (b) Simulation results with ±20% variations in capacitance. (c) Simulation results with parasitic parameters and integral compensation.

Figure 11b indicates that the Δi_L remains relatively stable despite the -20% variation in capacitance value, with all other nominal parameters held constant. However, a minor variation in Δv_o is visible. The reason is that the capacitor will discharge more quickly when the MOSFET is turned off, and then charge more slowly when the MOSFET is turned on. When the capacitance value is increased by 20%, there is a sudden drop in the output voltage. However, this dip is typically transient and settles down within a period of 0.4 ms, as depicted in Figure 11b. The reason for this drop is that the larger capacitance takes longer to charge up, and the inductor needs more time to transfer energy to the capacitor. As a result, the output voltage temporarily decreases until the capacitor is fully charged.

The simulation results substantiate that the controller is resilient against considered fluctuations in the converter's parameters. This exemplifies the controller's efficacy in maintaining system stability and performance consistency, even in the presence of variations in inductance and capacitance.

4.2.2. Parasitic parameters

Real-world inductors, capacitors, diodes, and MOSFETs exhibit various characteristics that must be considered during circuit design, such as inherent resistance, forward voltage threshold, and on-resistance. They also must be taking into account when designing a controller for a system. The simulation results shown in Figure 11c have considered the parasitic parameters outlined in Table 3. As depicted in Figure 11c, the presence of parasitic parameters leads to a considerable steady-state error. To mitigate this error, we introduce an integral compensation approach given by

$$u = K_I \int (V_{ref} - v_o) dt \ . \tag{12}$$

The compensation term u must be added to equation (10) to compose the final J. Here, unity integral gain is considered.

By implementing the suggested current reference compensation technique, the controller maintains its existing structure and switching conditions. Consequently, the system sustains stable performance, even when faced with uncertain system parameters, thus substantially enhancing its overall robustness, as shown in Figure 11c.

4.3. Comparison of the proposed scheme with PID and Fractional Order PID (FOPID) control

The design specifications are outlined as follows: $V_{in} = 24$ V, $L = 0.1$ H, $C = 47$ μF, $R = 25$ Ω, $f = 5000$ Hz, and $V_{ref} = 10$ V [8]. Table 5 compares the proposed control scheme with the existing PID and FOPID control schemes, while Figure 12 displays the state variables waveform. The analysis highlights the distinctions and potential benefits of the proposed approach. The proposed method exhibits superior efficacy in improving rise time and reducing overshoot and undershoot while maintaining a high slew rate. However, its potential disadvantage lies in the longer settling time required for the system to reach a steady-state value as compared to the FOPID scheme. Nevertheless, the benefits of enhanced performance justify the trade-off in settling time.

4.4. Limitations and future directions

The suggested control scheme is well-suited for buck converters operating in low to medium-switching frequencies. However, for the control scheme to yield optimal performance when the converter operates at higher switching frequencies, a higher sampling frequency is necessary since the control scheme heavily depends on a digital signal processor (DSP) to calculate the converter's switching times. To make an accurate estimation of the error and compute the switching times, the DSP must sample the output voltage

Parameter	PID [8]	FOPID [8]	Proposed Method
V_o(V)	9.933	9.99	**10**
Rise time (μs)	92.687	40.614	**2.943**
Slew rate (mV/ms)	85.735	105.223	**3863**
ΔV_o (V)	0.02	**0**	0.006
M_p (%)	15.698	0.505	**0.503**
Undershoot (%)	2	2.06	**1.997**
T_s (ms)	19.98	**0.003**	3.535

Table 5. Comparative analysis of the dynamic and steady-state performance of the proposed scheme with existing PID and FOPID scheme.

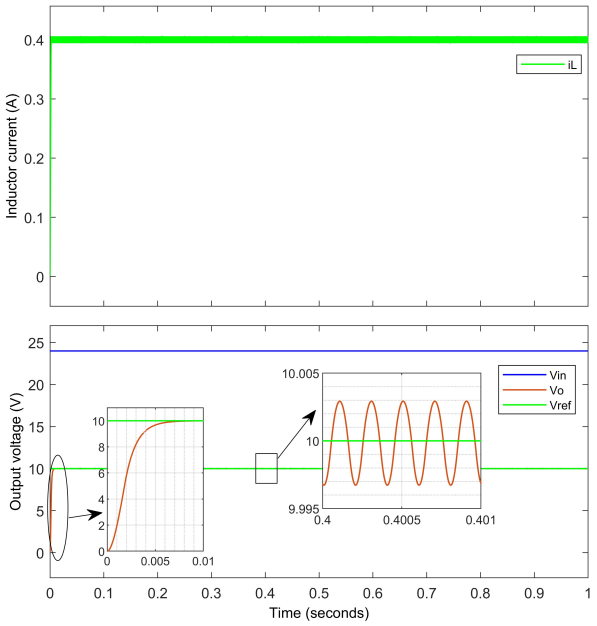


Figure 12. State variables of buck converter with the proposed scheme for comparison with existing PID and FOPID scheme

and inductor current at a high frequency. Consequently, high-speed ADC and a fast DSP are essential to attain the requisite sampling frequency.

To address the challenge of high switching frequency, one potential solution is to employ a Field-Programmable Gate Array (FPGA) to execute the control methodology. An FPGA is a versatile, programmable device capable of carrying out specific functions, such as control algorithms. Utilizing an FPGA enables the implementation of a control scheme that can function at high sampling frequencies while preserving low latency and high precision. Furthermore, FPGAs are readily reprogrammable, allowing control schemes to be adjusted and optimized as necessary. Thus, the adoption of an FPGA can surmount the constraints of the proposed system due to the requirement for high sampling frequency.

5. Conclusions

In this paper we proposed a boundary-based PWM control scheme for DC-DC buck converters operating in CCM. The approach utilizes SDS modeling of the converter circuit, enabling the implementation of a fixed-frequency PWM control scheme. Simulation results demonstrate the efficacy of the proposed control

scheme in achieving fast and accurate regulation of the output voltage while also exhibiting robustness to parametric variations. Furthermore, we found that incorporating integral compensation is an effective method for mitigating the impact of parasitic parameters in controller design. The controller's superior steady-state and dynamic response compared to other conventional control schemes make it an attractive option for controlling DC-DC buck converters in CCM. Overall, our proposed control scheme presents a straightforward and efficient solution for regulating DC-DC buck converters in CCM.

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